

# Strategy for enhancing reliability and lifetime of DC-AC inverters used for wind turbines

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## ABSTRACT

Lifetime of wind turbine inverters is below expectations therefore, novel design and drive strategies are timely required to achieve optimum life span.

In this work, a novel driving strategy to mitigate stresses on inverters is proposed. First, an electro thermal analysis was carried out using finite element modelling methods. Subsequently, the outcomes of the models were validated using DC/AC IGBT based power inverter module interfaced to 1.1 kW electrical outputs of a horizontal wind turbine operated under different wind speeds. Real time data was collected using both dSPACE system and high speed thermal imaging camera. The proposed driving method is based on adjusting the switching frequency according to wind speed. Edge detection scheme was embedded in Simulink to determine temperature fluctuations caused by variations in wind speed profile. Effects of these fluctuations are mitigated by regulating the switching frequency and power losses based on a look up table and interpolation method. The proposed strategy of operation reduces cyclic temperature depended lifetime span (total lifetime consumption) to  $1.45 \times 10^{-5}$  cycles compared to  $1.88 \times 10^{-5}$  when operated under conventional fixed frequency. Wire-bond thermal stress was also reduced from 54.5 MPa, for the fixed switching frequency, to 45.5 MPa. This represents about 21% reduction in total lifetime consumption of inverter's wire-bond which, brings huge benefits to wind energy industry.

## 1. Introduction

In wind turbines, power electronic converters (PECs) switching devices e.g. insulated gate bipolar transistors (IGBTs) have earlier break down mechanisms [1] compared to the other elements. This is caused by thermo-mechanical effects or long-term exposure to high temperatures during variable mission profiles [2] under changing weather conditions. IGBT modules consist of different layers as shown in Fig. 1, with different material properties. During its operation, temperature cycling generates stress within bonded materials which have different coefficient of thermal expansions (CTEs) [3]. This causes fatigue at regions such as bonding wire or solder; hence, degradations and eventual failures occur [4].

According to Lu et al. [6], almost 60% of failures are caused by temperature cycling. Two main failure mechanisms are solder fatigue and bond wire lift-off. Thermal resistance increment occurs due to the solder fatigue, and on-state voltage increment is commonly caused by the wire bond lift off [7]. Reconstruction of the aluminium metallization mostly initiates bond wire lift-off due to the plastic stress relaxation

of the aluminium. During power cycling, it causes increment in the collector to emitter voltage which results in higher power losses and hence increases temperature profile of chips [8]. This expedites the bond wire lift-off due to the stress caused by thermal expansion between wire bond and the chip [9]. A sample view of the wire bond lift-off can be seen in Fig. 2.

After an emitter wire lift off, the associated chip is no longer able to conduct the current; hence other bond wires are forced to conduct higher current. This also causes a continual lift off for the other wires as they may experience more current than they are capable of [9]. In order to detect such temperature induced failure occurring, accurate electro thermal modelling is essential. Proper thermal models with heat coupling effect analysis were considered in [10,11]. These works studied a thermal impedance matrix that was convenient for thermal coupling effect estimations and most suitable way to represent actual heat path through the device. Drofenik et al. [12] expanded the study proposed in [10] from air cooled to a water cooled heat sink model for a power module. Total of 2% maximum temperature difference was observed when compared between FEM and infrared camera estimations. An

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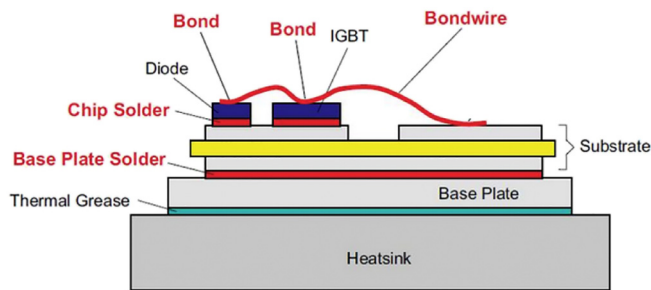


Fig. 1. Structural details of IGBT module [5].

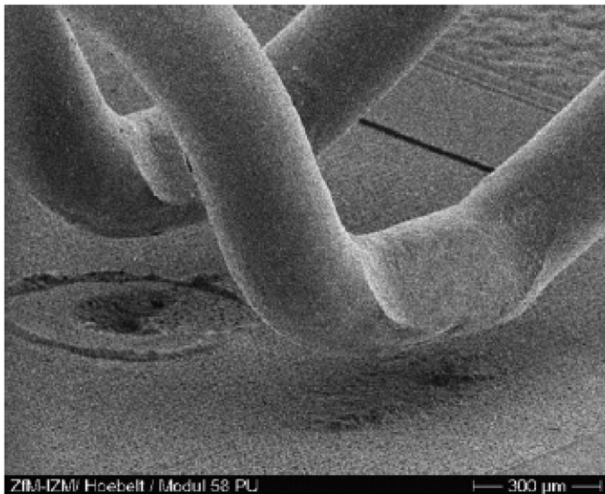


Fig. 2. Wire bond lift off mechanism [7].

experimental power cycling test proposed by Forest et al. [13] studied for ageing of IGBT power modules by monitoring device temperature and on-state voltage for detecting possible wire bond degradation and emitter metallization for the test devices IGBT modules. The average lifetime of the devices varied between 550,000 to 660,000 cycles and degradations were observed for the wire bond. von Mises stress was studied for analysing strain distributions due to thermal expansion and it was estimated that the highest stress occurred at the centre upper solder and gate bond wire [14]. Recently, Medjahed et al. [15] studied electro thermal stress for wire bonds of IGBT module located the maximal value (10 MPa) at the tail of the wire, near heel area where main failure modes occur close to this specific region. Description of power cycling experiments using the Joule heating of the bond wires for finding failures are presented in [16]. Ozkol et al. [17] studied power cycling performance of IGBT modules by implementing wire bond layout of the emitter contact.

Deriving accurate reliability prediction models are challenging due to the several reasons discussed in introduction and thermo-mechanical modelling sections [18]; hence, physics of failure approaches need to be investigated further by considering individual material properties and failure mechanisms of power module layer and interactions among themselves during power and thermal cycling. Xie et al. [19] proposed new failure models for power electronic converters used for wind turbines and confirmed that wind speeds and type of the generator have significant impacts on converter reliability performance [20,21]. Kostandyan and Ma [22] used rainfall algorithm to estimate temperature means and temperature variations. Palmgren–Miner rule [23] was used to calculate accumulated damage and to estimate reliability. This rule was also considered for deriving a reliability estimation method for solder joints of an IGBT power electronic module in [24].

Active thermal management systems are designed to regulate steady state and transient thermal-mechanical stress in power electronic

modules of operation [25]. Andresen and Liserre [26] analysed the thermal cycles of the junction temperature in dependence of current and switching frequency and they derived a switching utilization method for an electrical vehicle. Zhou et al. [27] proposed a novel method for reliability improvement of a inverter system. IGBT chip temperature was decreased from 9 °C to 0.5 °C based on the proposed model by carrier frequency adjustment through experimental implementation. Batunlu et al. investigated the reliability and thermal stresses of converters under different maximum power points tracking algorithms [28]. Based on the studied literature review, the switching frequency adaption method has not been applied to an actual wind turbine system based PEC. There is still need for evaluation of this method for thermo-mechanical stress and reliability analysis. In this paper, actual wind turbine was used to critically assess these method by interfacing a DC/AC IGBT based power inverter module. The electro thermal and thermo-mechanical test was performed by real-time application with dSPACE system. The case studies included a fixed and adjustable switching frequency of operation derived in [11]. The results were used to define total lifetime consumption (TLC) for the IGBT wire bonds.

The paper starts by state of art of the thermo-mechanical and electro thermal models for and recalling the proposed switching frequency adjusting technique in Section 2. In Section 3, experimental set up and critical assessments of the lifetime analysis are demonstrated and results are compared with the performance of conventional method. Conclusions are depicted in final section.

## 2. DC-AC inverters: function and operating methods

Inverters are needed to convert DC outputs of batteries or photovoltaic systems into an AC output voltage at desired frequencies and amplitudes. They mainly depend upon semiconductor switching devices such as insulated gate bipolar transistors or thyristors etc. These devices are derived by switching patterns such as square, sinusoidal pulse width modulation (SPWM) or space vector modulation (SVM) techniques; hence, although the output voltage waveforms of inverters should be sinusoidal, the waveforms of practical inverters are non-sinusoidal and contain certain harmonics. Their power loss characteristics also vary based on the type of the switching method used. Switching losses are affected by the driving frequency and the type of the switching method [11]. These losses are one of the main causes of the heat occurring on the inverters which cause high temperature profiles on these devices during operation. The conventional SPWM and variable frequency based proposed method to decrease the power losses are discussed in the following sections.

### 2.1. Sinusoidal pulse width modulation (SPWM) driving method

In SPWM, the generation of gating signals for a three phase DC-AC inverter with sine PWM are shown in Fig. 3. There are three sinusoidal reference waves ( $V_a$ ,  $V_b$ ,  $V_c$ ) each shifted by 120°. A triangular carrier wave ( $V_T$ ) is compared with the reference signals to produce the gating signals. The process is based on a constant switching frequency operation with the frequency modulation ratio ( $m_f$ ) is defined as the ratio between frequency of triangular signal ( $f_T$ ) and frequency of modulated sinusoidal signal ( $f_m$ ) which is used to modulate the switch duty ratio. In this study, a modified version of SPWM was proposed for a variable frequency operation and implemented in dSPACE RTI as explained in the following section.

### 2.2. Variable frequency driving method

The switching frequency of a PWM inverter affects the total switching power losses and hence temperature occurring on IGBT switches and antiparallel diodes as:

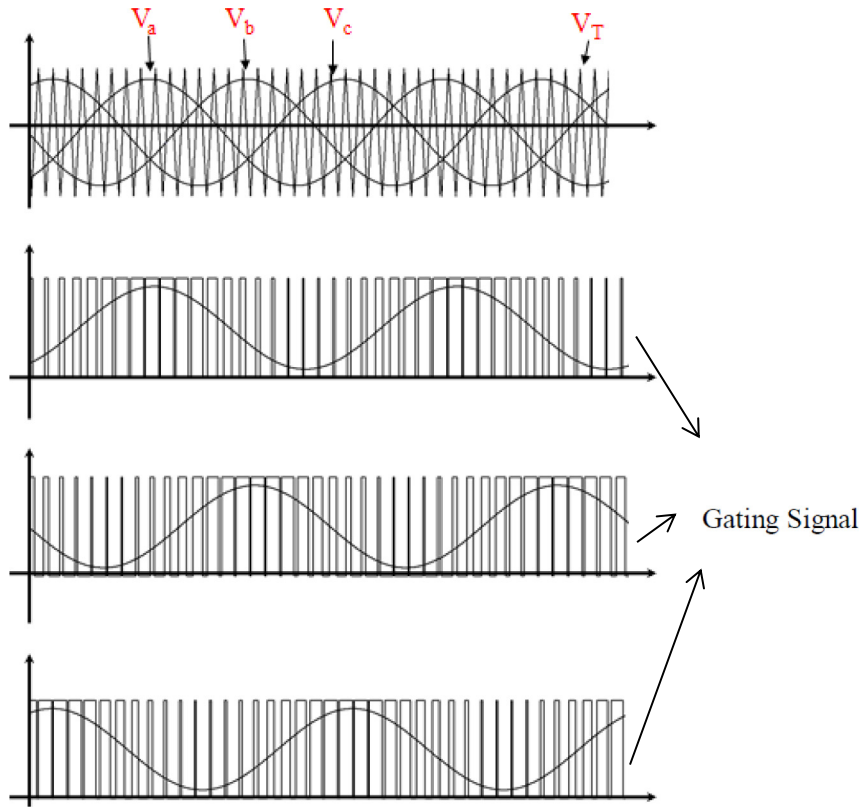


Fig. 3. Gating signal generation.

$$P_{SW,IGBT}(t) = f_s \cdot (E_{SW,ON}(I_C(t)) + E_{SW,OFF}(I_C(t))) \quad (1)$$

$$P_{SW,DIODE}(t) = f_s \cdot E_{SW,RR}(I_F(t)) \quad (2)$$

where the  $P_{SW,IGBT}$  is the instantaneous switching power losses of IGBT,  $E_{SW,ON}$  and  $E_{SW,OFF}$ , are the turn-on and turn-off energy losses,  $I_c$  is the IGBT collector current,  $I_f$  is the forward current across the diodes,  $E_{SW,RR}$  is the recovery energy losses of the diode and  $f_s$  is the switching frequency. One of the main concerns for the reliability issue for the semiconductor based inverter is the temperature swing (fluctuations) rather than the mean temperature itself as it is further discussed in the following sections. Therefore, the proposed method aims to minimise these fluctuations by considering the power losses and mean temperature. As it is stated in [11], for a kilowatt level inverter used in a wind turbine system, the temperature fluctuations can be kept constant by lowering the switching frequency around 50%, in the case approximately current increases 25%. In opposite case, where the current decreases, the switching frequency can be increased to keep the temperature fluctuations constant. However, in the latter, the mean temperature certainly increases as the frequency increases. Therefore, a limiter for the increment operation of switching frequency needed to be defined. For the purpose of controlling the temperature fluctuations, the flowchart of the proposed control strategy can be seen in Fig. 4.

The algorithm begins by measurement of energy losses as a function of current, voltage and temperature, in previously defined look up tables. Then power losses that are the input for thermal model are calculated as a function of switching frequency. When the current and the temperature swing both decreases the mean temperature is stored as a limiter value ( $T_{mo}$ ). Then the switching frequency is increased, by the ratio of K (ratio of modulation and carrier frequencies in multiple of three in order to keep each three-phase voltages in symmetric), as the stored and instantaneous mean temperature difference is lower than 3 °C. This value is selected as an example case for the purpose of limiting the mean temperature which can increase as the frequency

inclines. In the case of current and temperature fluctuation increment, the switching frequency decreased by the same ratio of K, as the temperature swing is higher than the previous sample data. The process is implemented by using edge detecting block available in Simulink Library.

### 3. Modelling and numerical simulation

The proposed method was applied to an actual permanent magnet generator based wind turbine system test rig. A double bridge AC/DC rectifier was used to convert the generated AC into DC. Then, the power module was used as an inverter during variable environmental conditions in order to analyse the performance of the reliability of the bond wires located on IGBT and diode chips. The studied inverter module for this study can be seen in Fig. 5(a) along with its circuit configuration which consists of six IGBTs and six diodes in Fig. 5(b).

The specifications of the module are presented in Table 1. The energy loss distribution over the device was calculated by a datasheet study using the methods studied as in [28]. Hence, the module losses were extracted to calculate the losses for each chip.

An enhanced version of the driver circuit derived in references [29,30], was implemented in order to drive the inverter module. 3-Phase/6-channel PWM feature of the DS5101 platform was used to generate gate signals. Then, the implemented driver circuit was used to increase to power level of these signals for sufficient gate driving.

#### 3.1. Finite element modelling

FE model of the inverter module was studied in details by using COMSOL. In order to increase the accuracy, dimension and material properties of each layer as well as the geometrical shapes of the wire bonds were accurately designed. The meshed view of the inverter model with the attached heat can be depicted in Fig. 6. The geometry

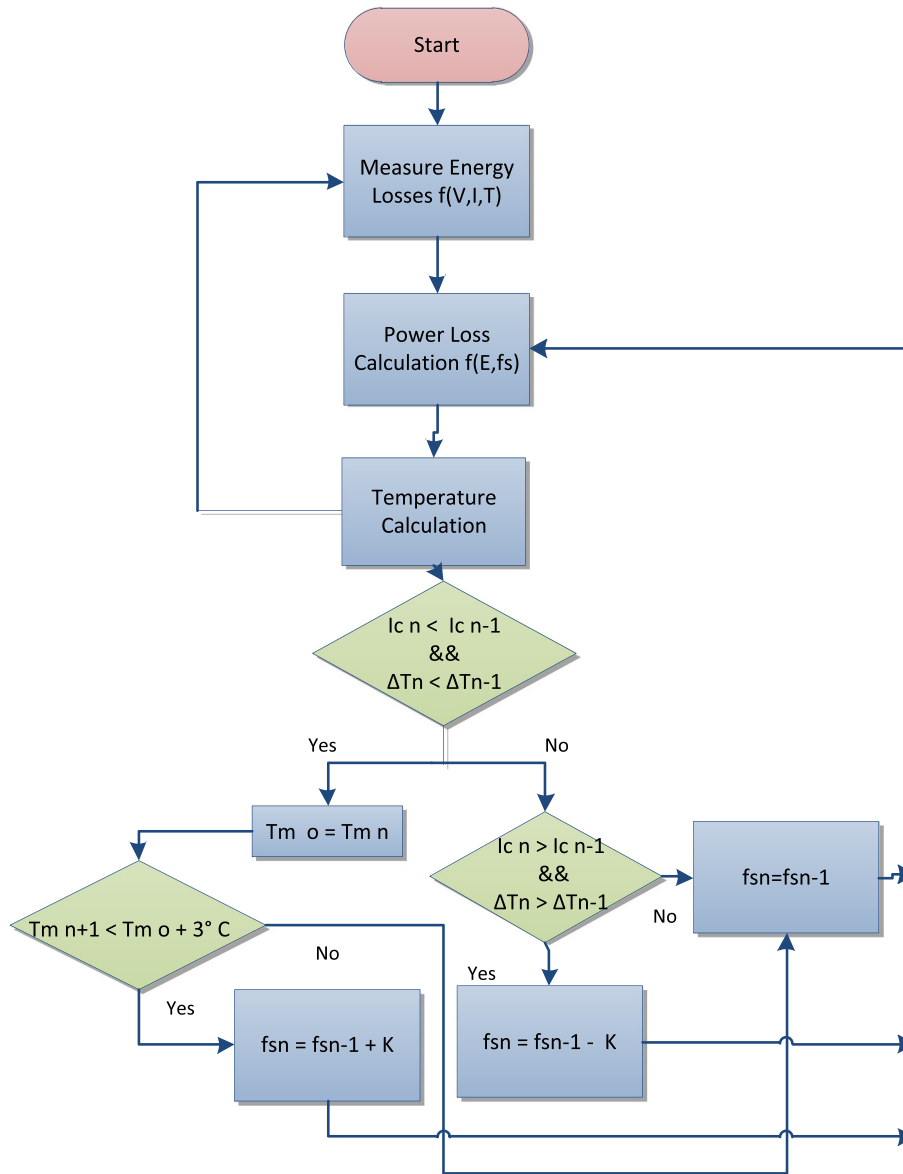


Fig. 4. Flowchart of proposed strategy.

was modelled with 111,743 tetrahedral elements. Mesh size for the heat sink and individual layers of the module are different for computational efficiency. Mesh refinement was completed by scale factor of two especially only for narrow edges of wire bonds and thin solder layers.

In the model, thermal conductivity properties are defined as a function of temperatures and considered as dynamic functions. Heat diffusion equation was defined for whole model to solve the distribution of temperature variations. It is defined as:

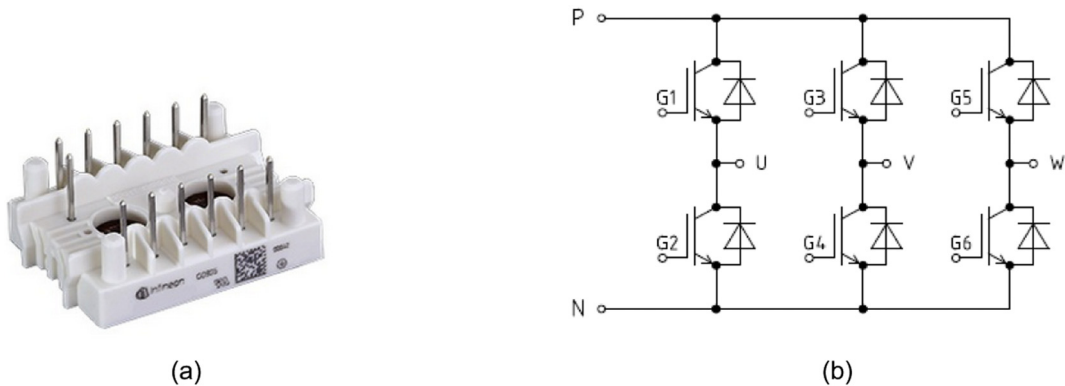
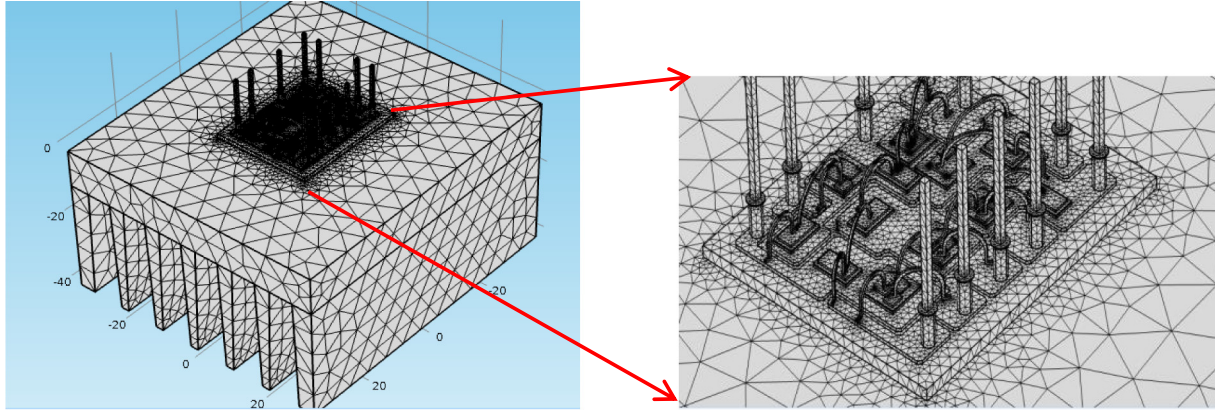


Fig. 5. (a) View of the inverter and (b) circuit configuration of the inverter.

**Table 1**  
Specifications of the inverter module.

Spec.	$V_{CEs}$	$I_{C(T=25^{\circ}C)}$	$I_{C(T=80^{\circ}C)}$	$C_{ies}$	$C_{res}$	$t_{d(on)}$	$t_r$	$t_{d(off)}$	$t_f$	$E_{on(T=25^{\circ}C)}$	$E_{off(T=25^{\circ}C)}$
Value	1.2 kV	16 A	10 A	0.70 nF	0.026 nF	0.037 $\mu$ s	0.02 $\mu$ s	0.29 $\mu$ s	0.09 $\mu$ s	0.95 mJ	0.7 mJ



**Fig. 6.** Meshed FE model of the inverter.

**Table 2**  
Physical properties of each layer material at 25 °C.

Layer	Physical properties at 25 °C					
	$\rho$ (kg/m <sup>3</sup> )	$k$ (W/mK)	$c$ (J/kgK)	CTE (10 <sup>-6</sup> /K)	Young modulus (MPa)	Poisson ratio
Silicon	2330	153	703	3.61	113.000	0.28
Solder	7360	33	200	30.20	27.557	0.40
Copper	8850	398	380	17.30	128.000	0.36
Alumina	3965	35	730	6.5	170.000	0.22
Aluminium	3300	180	750	4.60	344.000	0.22
Solder	11,300	35	129	29	16.876	0.44
T. grease	2500	2	700	29	15.700	0.32
Heat sink	2730	155	893	4.30	384.000	0.30

encapsulation silicone gel was removed. Hence, thermal isolation is no longer provided for the inverter module. In order to provide these test conditions in experimental analysis, the heat transfer coefficient  $h$  is defined as 5 W/m<sup>2</sup>K over the model representing the natural convection. Thermal and mechanical properties of the materials used for the FEM simulation are shown in Table 2.

The ambient and heat sink temperatures were set to be 20 °C. Each chip was heated, in individual simulations, by a constant two dimensional 10 W heat source. Heating operation for a diode chip can be seen in Fig. 7(a) & (b) at top surface and middle of the chip, respectively.

Transient thermal resistance  $R_{th}$  and thermal capacitance  $C_{th}$  for each layer was represented with Foster model [11] as follows:

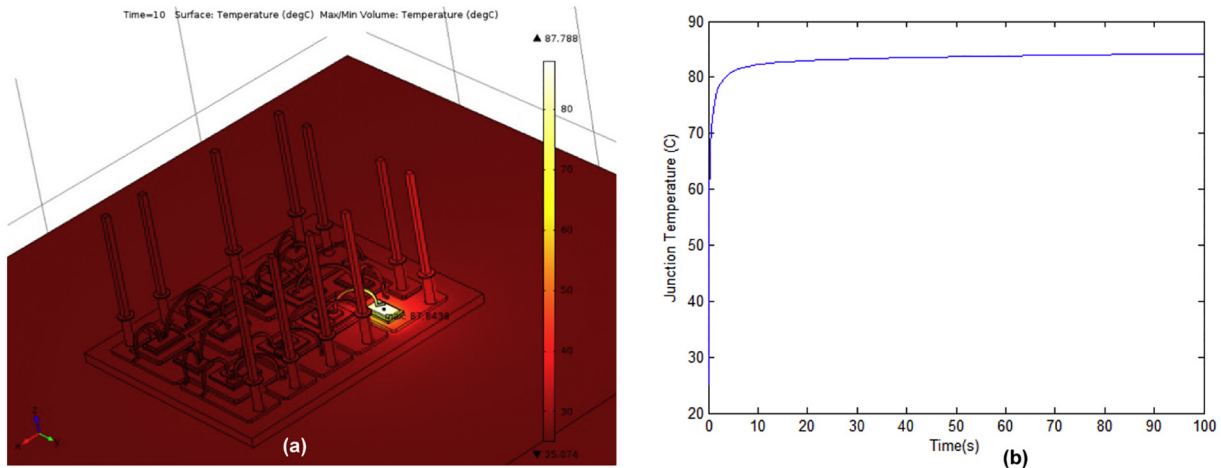
$$Z'_{th}(s) = R'_{th} / (1 + sC'_{th}) = \frac{R'_{th}}{sR'_{th}C'_{th} + 1} = \frac{1/C'_{th}}{s + 1/\tau} \quad (4)$$

where;  $\tau = R_{th}C_{th}$  (5)

$$\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} + \frac{q}{k} = \frac{\rho \cdot c}{k} \frac{\partial T}{\partial t} \quad (3)$$

where  $T$  is the temperature,  $k$  is the thermal conductivity,  $c$  is specific heat capacity,  $\rho$  is the mass density and  $q$  is the rate of generation of energy per unit volume. The module was unmounted and the

In order to extract the thermal impedance parameters, the methodology defined in [29] was followed. Then, the thermal impedance matrix was implemented as in [11] based on the self-heating and cross coupling heat generations among each neighbouring chips. For  $M$  layers



**Fig. 7.** Heating operation of diode chip of inverter at a) top surface and b) middle.

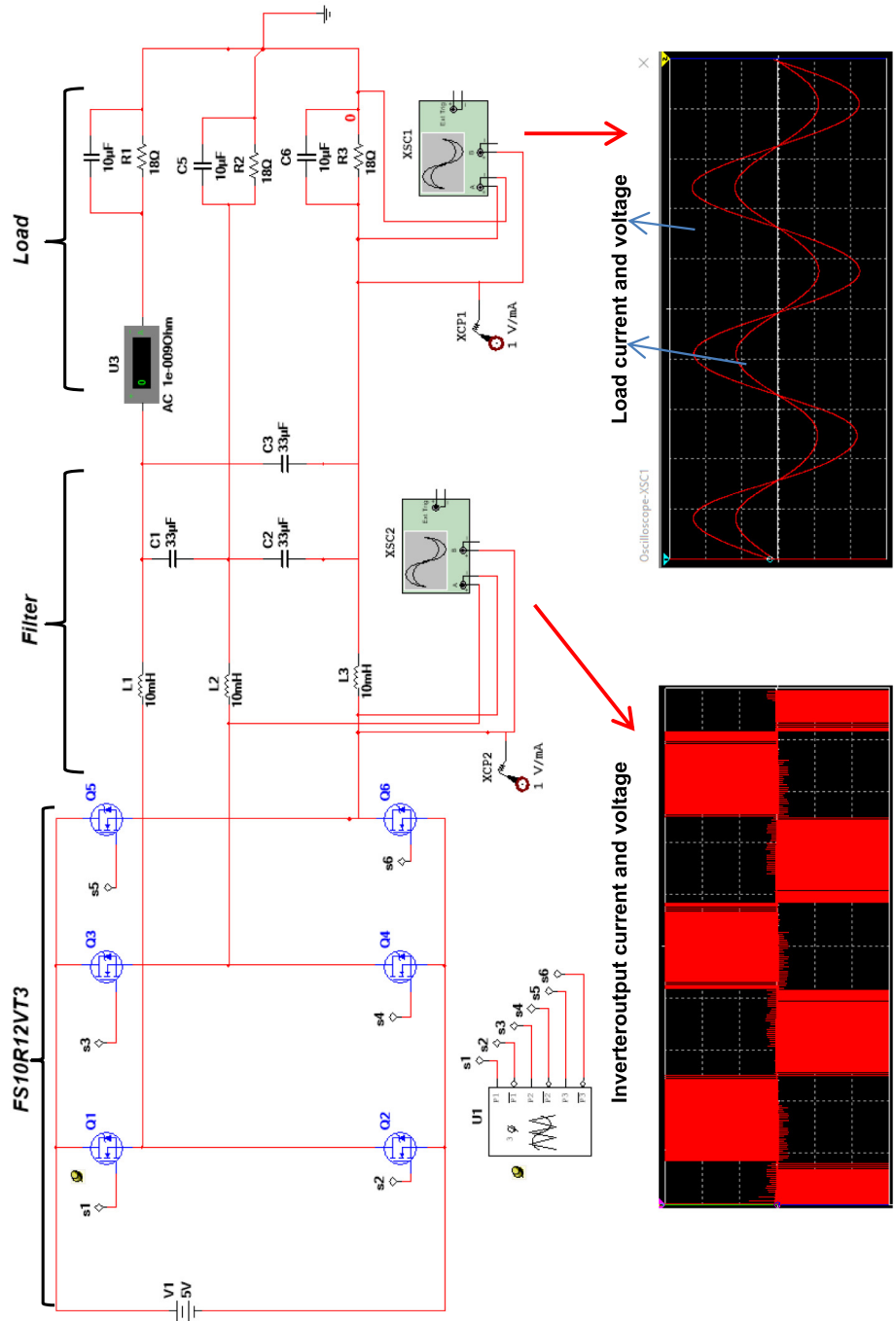


Fig. 8. View of the multism model.

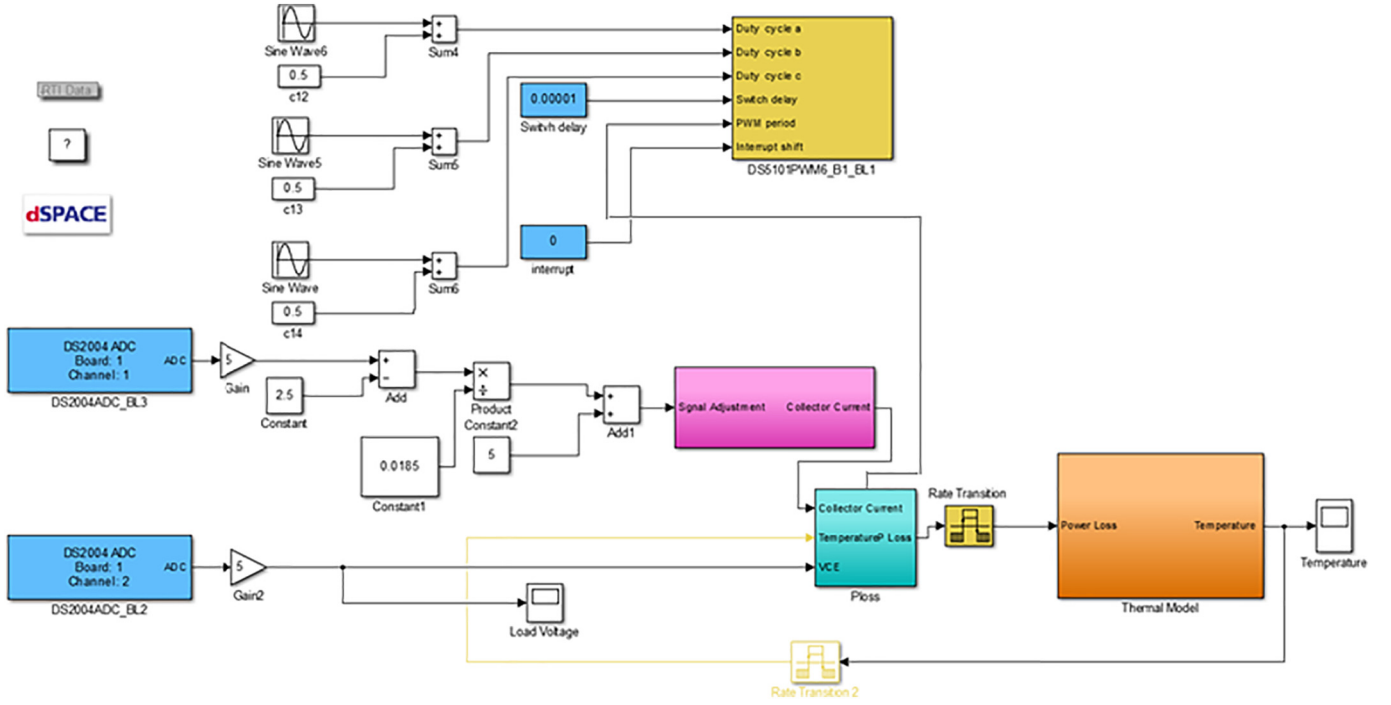


Fig. 9. dSPACE implementation.

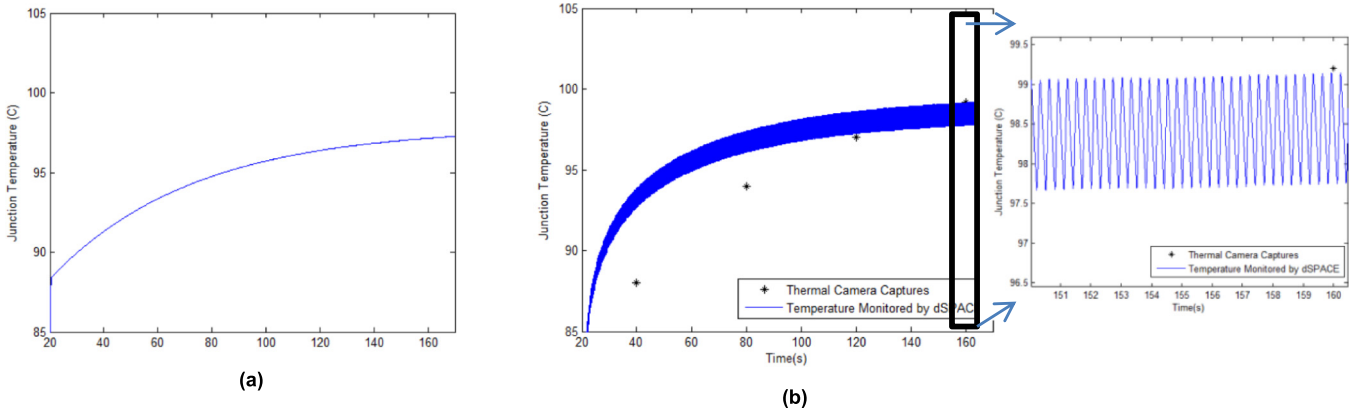


Fig. 10. Temperatures observed by (a) Simulink model and (b) by dSPACE and thermal imaging.

and  $n$  heating sources, the temperature of each layer can be expressed as:

$$T_m(s) = \sum_{n=1}^N \sum_{k=1}^{Kmn} \frac{A_{mnk}}{s + \alpha_{mnk}} P_n(s) \quad (6)$$

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{jN} \\ T_{solder1} \\ \vdots \\ T_{AI1NN} \\ \vdots \\ T_{baseplate} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1N} \\ a_{21} & a_{22} & \cdots & a_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ a_{N1} & a_{N2} & \cdots & a_{NN} \\ \vdots & \vdots & \ddots & \vdots \\ a_{M1} & a_{M2} & \cdots & a_{MN} \end{bmatrix} \begin{bmatrix} P_{in1} \\ P_{in2} \\ \vdots \\ P_{inN} \end{bmatrix} + T_0 \quad (7)$$

where  $A$  is the coefficient  $1/C_{th}$  and  $\alpha$  is the  $1/\tau$  in Eq. (4). A matrix form of Eq. (4) can be derived as in Eq. (7) where  $a_{11}, \dots, a_{MN}$  are the transfer functions of thermal impedances.

### 3.2. Electrical circuitry modelling

Multisim software was used for filter design of the three phases. The aim of this paper is not to design an optimised filter for the inverter module. Nevertheless, for accuracy of the real time (RT) electro thermal measurements, appropriate sinusoidal current and voltage signals are needed in terms of harmonic distortion. A conventional, second order LC filter was implemented to reduce harmonic distortions caused by fundamental square waved output voltage of the inverter. A shunt capacitor is used to further attenuation of the switching frequency components [31]. It is selected to produce low reactance within the control frequency range. The resonant frequency is calculated from Eq. (8).

$$f_s = \frac{1}{2\pi} \cdot \frac{1}{\sqrt{LC}} \quad (8)$$

where the  $L$  is the inductance,  $C$  is the capacitance at selected switching frequency  $f_s$ . The characteristic impedance of the passive filter  $Z$  is given by:

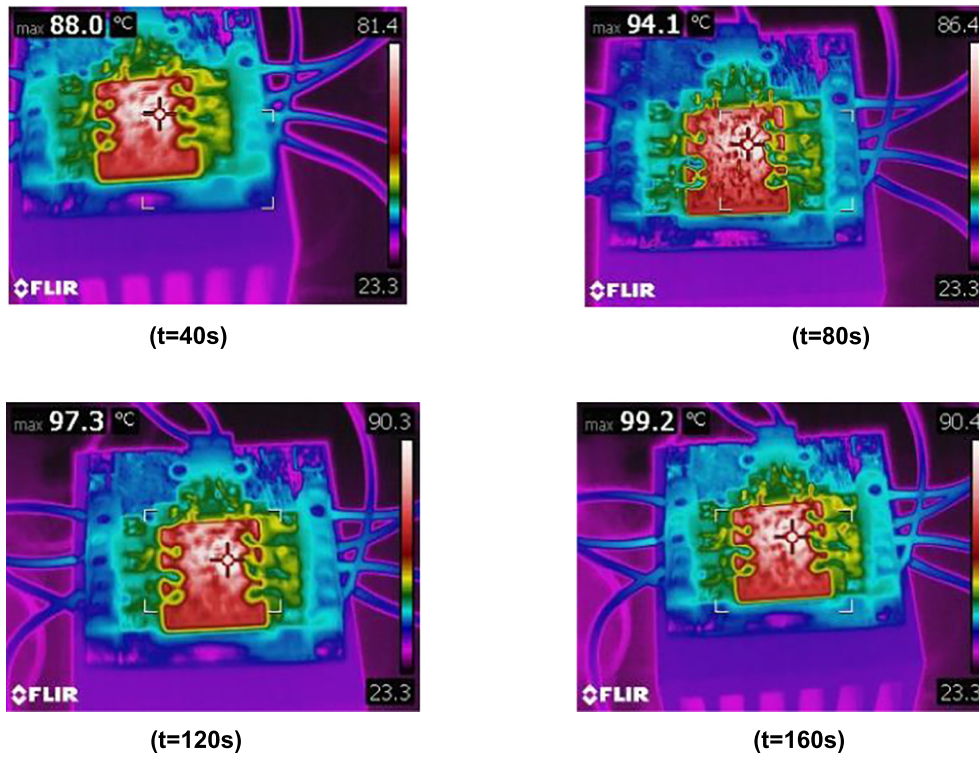


Fig. 11. Thermal camera captures.

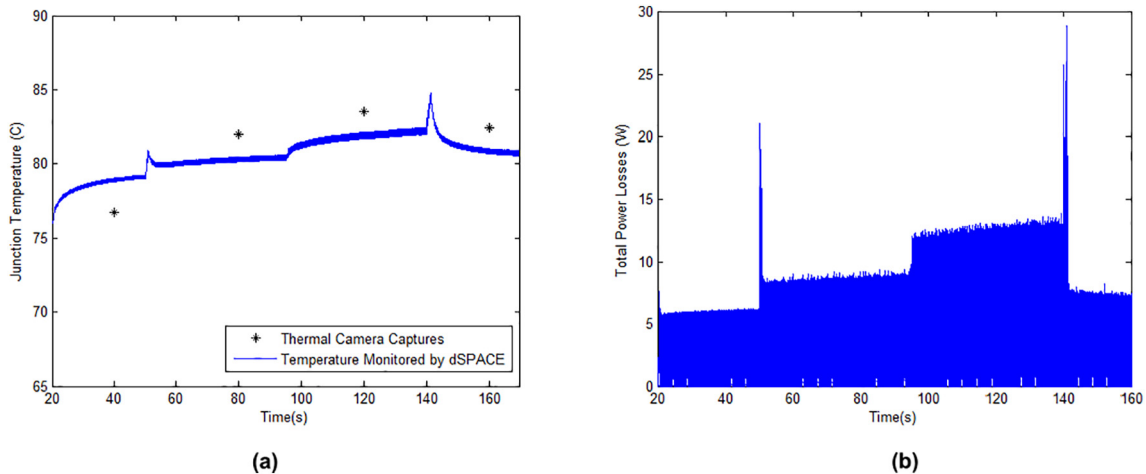


Fig. 12. (a) Temperature observed by dSPACE and thermal imaging, (b) power losses.

$$Z = \sqrt{\frac{L}{C}} \tag{9}$$

The impedance,  $Z$  determines filtering performance at harmonic frequencies except for the resonant frequency. Lower characteristic impedance reflects a lower DC capacitor voltage as well as lower EMI emissions [32]. The modelled 3-phase inverter systems can be depicted in Fig. 8. As filtering, 10 mH inductors and 33  $\mu$ F capacitors were selected along with the available 18  $\Omega$  resistors and 10  $\mu$ F capacitors as balanced loads.

#### 4. Experimental setup and results

The heat sink, with dimensions of 75  $\times$  66  $\times$  40 mm, was mounted on an isolated mica platform along with the driver circuits. In order to mount the input and output terminals of the inverter module, a PCB

circuit was implemented and soldered to the specified legs. The inverter is isolated through the middle gap of the PCB circuit and mounted directly on the heat sink. A total of six gating circuits have been implemented for driving six individual gate signal provided by DS5101 DAC platform. A combination of gate driver and opt coupler, namely the HCPL-4502 and TD3511D was designed. The DS5101PWM6 block from dSPACE Control desk was used to generate SPWM based gate signals for each IGBT as shown in Fig. 9. The collector current and voltages were captured by the DS2004 A/D platform and processed in to power loss and thermal models. A case study was conducted at constant 5 V volt input while the switching frequency of the SPWM was 100 kHz.



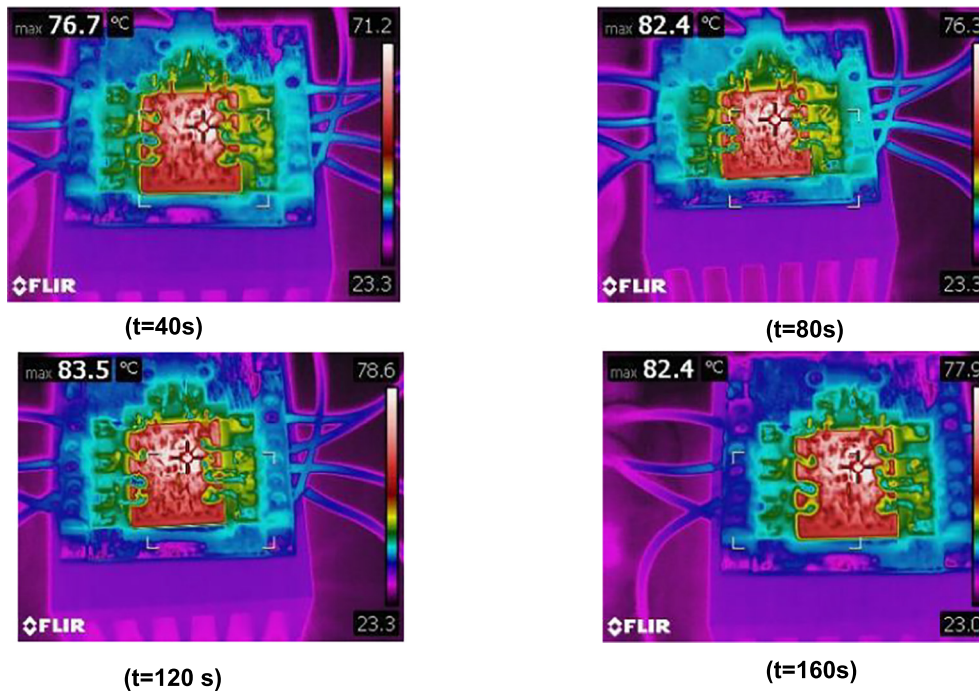


Fig. 13. Thermal camera captures.

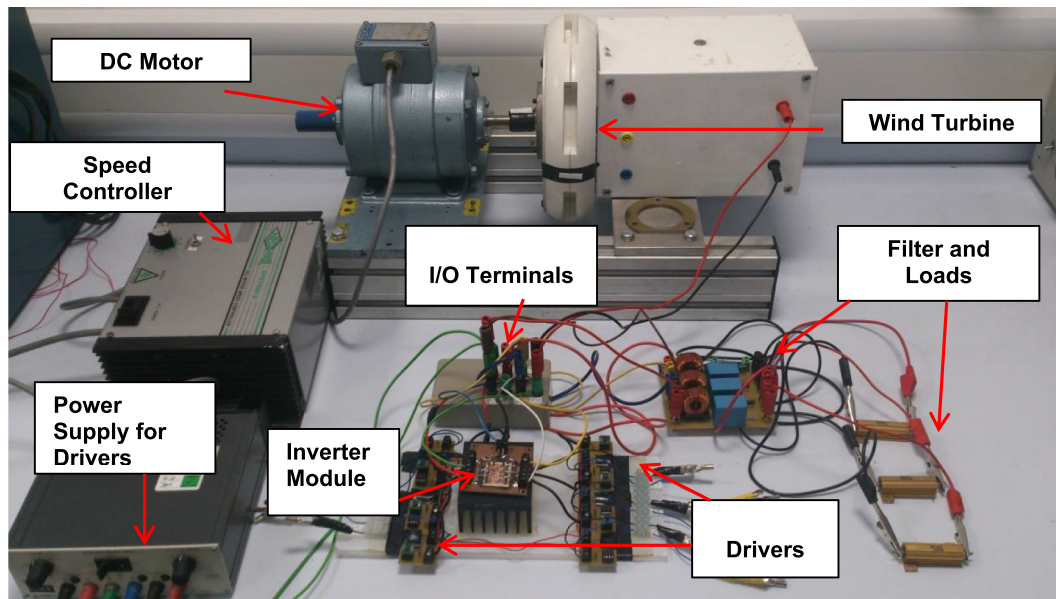


Fig. 14. Physical view of the experiment.

#### 4.1. Electro thermal modelling results

The electro thermal modelling methodology derived in [11] was applied to the inverter module by considering self and coupling effect among each chip. IGBT and freewheeling diode current and voltage signals are directly embedded in power loss models for each device. The temperatures for each layer were monitored by feedback look through individual thermal layer model. Results are depicted in Fig. 10(a) & (b) for simulated and experimental studies, respectively.

The input DC voltage was adjusted as 5 V where the switching frequency was 50 kHz. The maximum temperature reached up to 96 °C for the simulated case. Compared to the individual heating operation seen

in Fig. 7(b), by the electro thermal model in Simulink, 15 °C temperature increase can be obtained by considering the heat coupling effect. The experimental results are also in good agreement with the simulated data as seen in Fig. 10(a). The thermal imaging captures were taken in 20 s of intervals (see Fig. 11) while the dSPACE model predicts the instantaneous temperature based on the load current and voltage. Approximately 1.5 °C temperature swing was estimated during the inverter operation, as well. The electro thermal modelling method was considered as successful based on these observations.

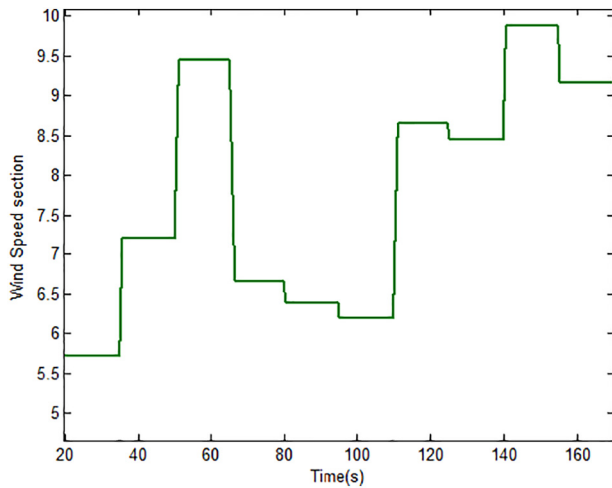


Fig. 15. Wind speed profile.

#### 4.2. Effectiveness of proposed switching strategy

A variable temperature profile was generated by varying the switching frequency at constant input voltage. Four sets of different SPWM switching frequency were applied to the inverter in 20 s intervals. The monitored temperature along with the power loss data can be in Fig. 12(a) & (b), respectively during variable switching frequency operation. The initial switching frequency was 10 kHz and it was increased to 50 kHz and 100 kHz in each 20 s. Then, the frequency was pulled back to 20 kHz at 140 s.

The power losses increased as the switching frequency increased and this reflected on the instantaneous temperature where it was at its highest, 83 °C at 100 kHz due to the higher switching losses. Thermal camera captures in stated time intervals can be seen in Fig. 13.

By these experimental results, the arguments in [11,27] are verified in terms of switching frequency variation and its effect on the temperature changes. The higher switching frequency led higher power losses at specified time intervals which caused temperature increments and vice versa. The distortion of the output voltages at various switching frequency rates also explains the total harmonic distortion variations where it was the worst at 10 kHz of switching frequency and was smoother as the switching frequency increases.

#### 4.3. Real-time reliability estimation

The obtained results were practically verified using the experimental set up shown in Fig. 14. The experimental set up consists of 1.1 kW permanent magnet generator, AC-DC rectifies, DC-AC inverter module and other auxiliary units. The generator was operated using the speed range profile shown in Fig. 15. When wind speed increases, switching frequency is adjusted according to losses. Temperature profiles for both operation along with temperature variations shown in Fig. 16(a) & (b). For the fixed frequency operation the system was operated under 50 kHz with fixed switching frequency. As shown in Fig. 16, inverter's temperature increases when wind speed increases. The highest estimated temperature was 85 °C at the speed portion of 10 with fixed frequency operation whereas 80.5 °C with the adjusting operation. The thermal profile behaviour increased with respect to the increments in wind speed as the defined in [11].

Higher energy produced by the wind turbine generator caused more power losses which results in higher temperature profile for the inverter module at high wind speeds. In both cases, the temperature fluctuations which are main cause of thermal stress and fatigue also were increased with higher wind speeds; however, the adjusting operation provided smother intervals during these changes. The power losses due to the sudden voltage/current changes are declined by the control method. The mean temperature also lowered by approximately 5 °C at 140 s. The gate signals were provided by dSPACE and the converter current was used to predict the power losses processed through the look up tables and to calculate the inverter temperature during the variable speed profile.

#### 4.4. Stress estimation and prediction of remaining life

The recorded power losses for both fixed and regulated switching frequency operations were the inputs for finite element models to calculate von Mises stress occurs on chip wire bonds. Yielded stress distribution is by Eq. (10).

$$F = \sigma_{Mises} - \sigma_{yield} \tag{10}$$

where  $\sigma_{yield}$  is the yield stress and  $\sigma_{Mises}$  is the von Mises stress which is calculated by Eq. (11).

$$\sigma_{Mises} = \sqrt{\frac{3}{2} dev(\sigma): dev(\sigma)} \tag{11}$$

where  $dev$  is the deviatoric stress tensor. The behaviour of solder layers including temperature sensitivity is calculated using the method presented in [33]. Resulted stress is shown in Fig. 17(a) & (b). Wire bond

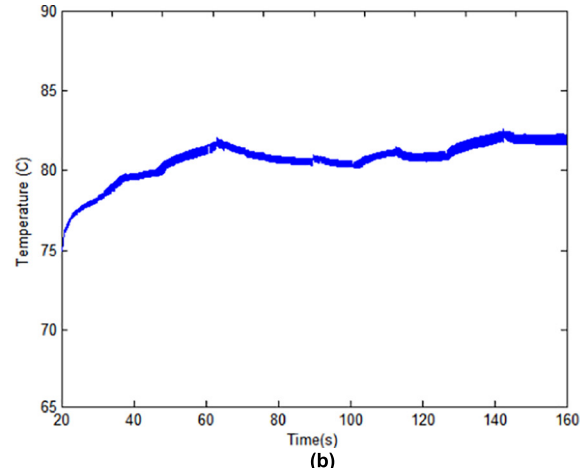
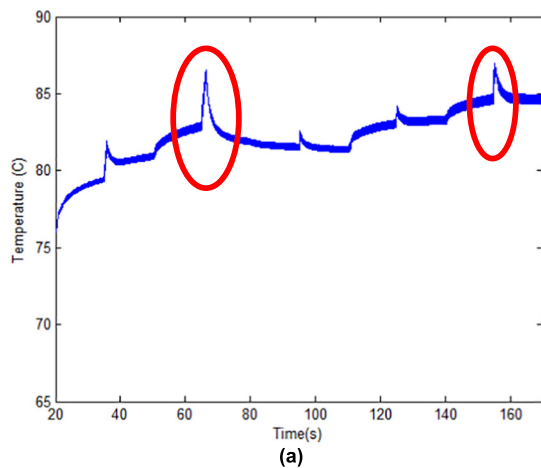


Fig. 16. Inverter temperature with (a) fixed frequency and (b) adjustable frequency.

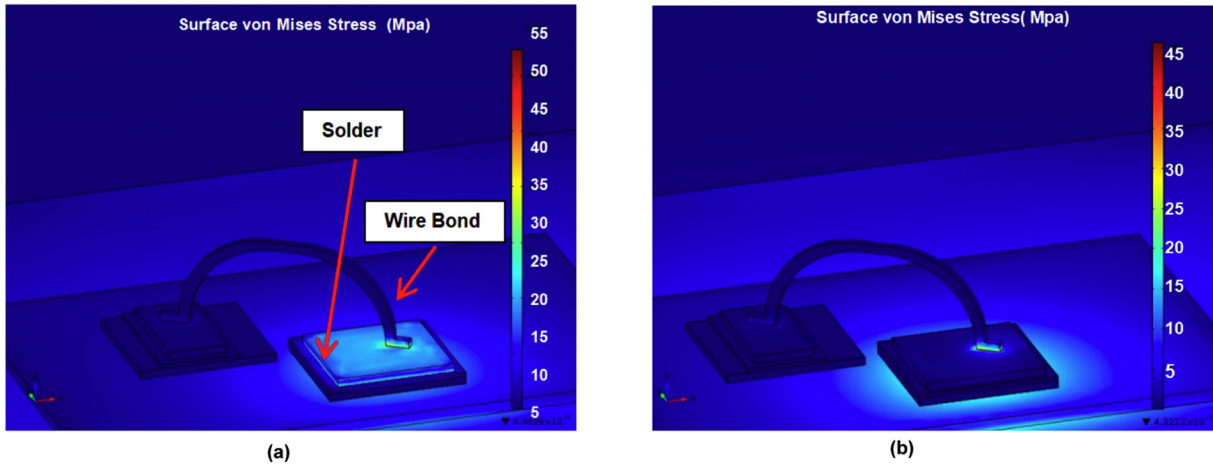


Fig. 17. Surface von Mises stress for (a) fixed and (b) regulated switching frequency operations.

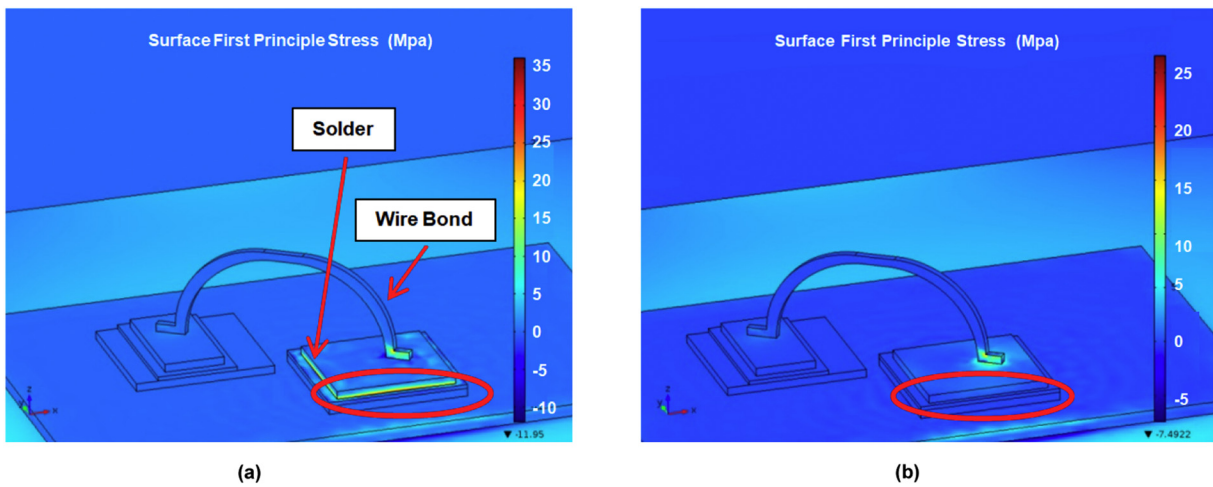


Fig. 18. Surface first principle stresses for (a) fixed and (b) regulated switching frequency operations.

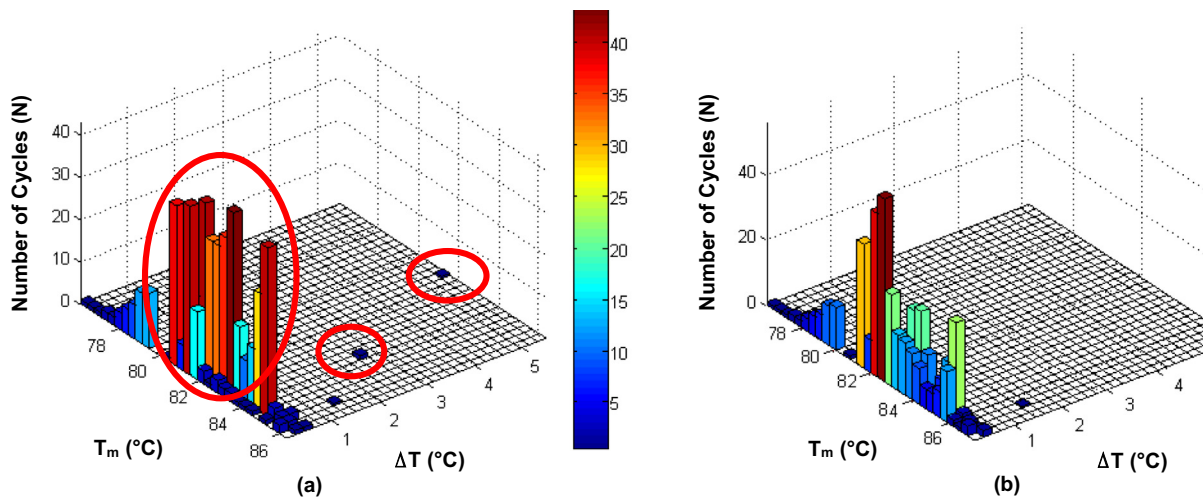


Fig. 19. Rain flow thermal cycling data for (a) fixed and (b) regulated switching frequency operations. (For interpretation of the references to colour in this figure, the reader is referred to the web version of this article.)

layers and silicon solders are the most stress affected parts. The maximum von Mises stress is found to be at the contact points between the wire bonds and the silicon layers which causes lift as defined in [7,9].

Wire bond stress was estimated to 54.5 MPa where it was 38 MPa for solder layer, 27 MPa for the silicon chip and 19 MPa for baseplate for

the fixed switching frequency. The wire bond stress was mitigated from 54.5 MPa to 45.5 MPa by the proposed method. Approximately 9 MPa less stress was achieved with the proposed scheme compared to conventional fixed method. Stress across the upper layer of the chip caused by highly cycling temperature profile with the fixed switching

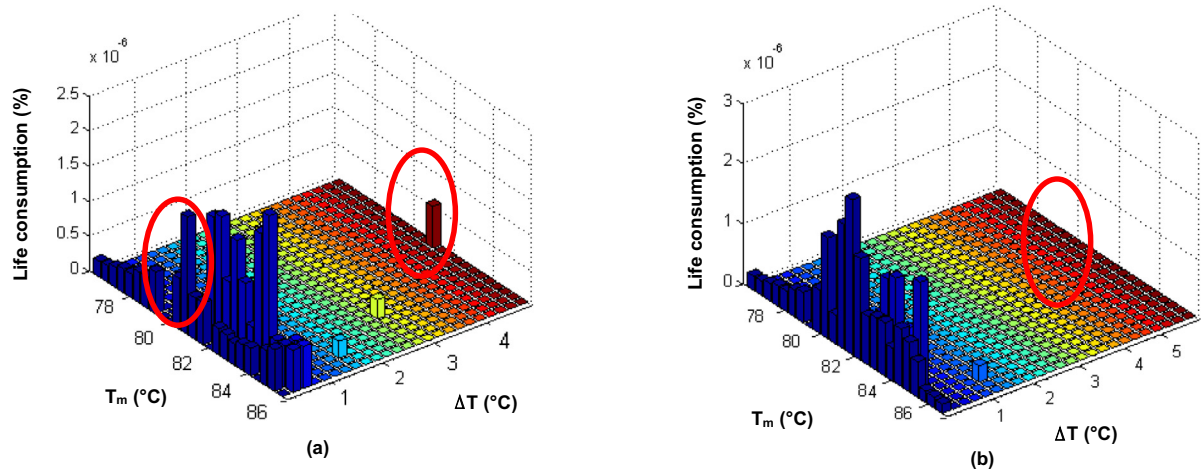


Fig. 20. Lifetime consumption during variable speed for (a) fixed and (b) regulated switching frequency operations. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

frequency operation of the inverter is decreased with the proposed method, as well. Stress across silicon layer edges and copper is reduced in overall. First principle stress analyses are shown in Fig. 18(a) & (b) for each method.

A 26.4 MPa stress was induced using the proposed method compared to 36.1 MPa caused by the usual method of operation. Moreover, thermal stress distribution with fixed method is worse than that caused by the proposed driving method due to highly fluctuated characteristics. Solder layer stress also decreased at the contact area with the silicon layers which reduces crack failures.

#### 4.5. Inverter reliability investigations

Lifetime estimation methodology discussed in [5], was used to calculate thermal cycles and predict life consumption (TLC) of wire bonds. The expected number of cycles to failure is calculated using Eq. (12):

$$N_f = 4 \times 10^{17} \cdot \Delta T^{-6.48} \quad (12)$$

A 3-D graph to represent effects of mean temperature ( $T_m$ ), temperature variation ( $\Delta T$ ) and total temperature cycles ( $\Delta T$ ), calculated using rainflow counting algorithm [34], is shown in Fig. 19.

The high numbers of cycles at mean temperature between 80 °C to 84 °C in Fig. 19(a) were massively reduced in Fig. 19(b). To be more quantitative, at  $\Delta T$  3 °C and 5 °C (shown in red circles in Fig. 19(a)), correspondent mean temperatures were 84 °C and 81 °C respectively. While in Fig. 19(b), those fluctuations are mitigated by the proposed driving method. Therefore, effectiveness of the proposed method is clearly demonstrated by remarkable decrement in number of cycles compared to the conventional method of operation.

This high fluctuation in temperatures causes more stress, speeds up failures reaching points and leads to reductions in lifetime.

Total lifetime consumption, shown in Fig. 20, was calculated using linear damage accumulation method from reference [35]. TLC of inverter's wire bond was decreased to  $1.45 \times 10^{-5}\%$  compared to  $1.88 \times 10^{-5}$  in the case of conventional fixed frequency operation. About 21% less TLC was achieved with the proposed method under same loading and environmental conditions compared to the conventional one. This is clearly shown in areas identified by red circles. Much less TLC was achieved using the proposed method (shown in Fig. 20(b)) e.g. at TLC is about  $0.5 \times 10^{-6}$  at  $\Delta T$  of 5 °C and  $T_m$  of 81 °C using conventional driving method compared to  $0.001 \times 10^{-6}$  with the proposed method.

## 5. Conclusion

An effective driving method, to extend lifetime of DC-AC inverters, have been proposed and experimentally verified. The proposed switching frequency method reduces inverter's wire-bond total lifetime consumption by about 21%. Total lifetime consumption of  $1.88 \times 10^{-5}$  with conventional fixed frequency operation was effectively reduced to  $1.45 \times 10^{-5}$  with the proposed driving method. This has been verified using finite element modelling and data collected from a wind turbine system while working under realistic operating conditions.

The total von Mises stress, occurring at the wire-bonds of the inverter, was decreased from 54.5 MPa for the fixed switching frequency to 45.5 MPa with the proposed controlled frequency operation method. The possible drawback for the proposed method could be the visible distortions on the sinusoidal current and voltage signals. These could be minimised by keeping fixed ratio between fundamental and carrier frequencies and can be further eliminated by active filtering methods in further studies. It is believed that the proposed method is now ready to be adopted by industry.

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