



A CMOS transimpedance amplifier with high gain and wide dynamic range for optical fiber sensing system



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ABSTRACT

For the optical fiber sensing applications, a new CMOS transimpedance amplifier (TIA) with high gain and wide dynamic range has been designed based 0.18 μm CMOS process. The TIA proposed consists of three-stage cascade push pull inverter, inductive-series peaking, automatic gain control (AGC) circuit, signal to differential circuit, and output buffer. Three-stage cascade push pull inverter is used to achieve enough high gain. The inductive-series peaking technique is employed in this design to extend further the bandwidth. Automatic gain control circuit is used to realize wide dynamic range. In order to reduce the signal reflection, output buffer is added in this design. Owing to the signal output of three-stage cascade push pull inverter and the differential inputs of output buffer, Single to differential circuit must be set in the design to complete the matching.

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1. Introduction

Recently, a method of using an optical fiber as a sensor for detecting, for example, ground deformation, the distortion or deformation of a structure, etc., has been proposed. Fig. 1 shows the optical fiber sensing system which mainly includes optical source, transmission optical fiber, sensing head, photodetector, and signal processing module. In this system, a transimpedance amplifier (TIA) is used widely as the front-end of signal processing module to convert the small photocurrent from the photo-detector to an amplified voltage signal. Therefore, the TIA has better possess a high gain. At the same time, it should have a wide dynamic range (DR) and low noise because the large input photocurrent saturates the TIA and makes it insensitive to the input signal [1].

To process the weak photocurrent signal, TIA gain is needed to be large enough. In practical optical fiber sensing applications, the TIA does not always operate a nearby sensitive case, i.e., handling the lowest input signal considered. When high input signals are processed, saturation might occur and degrade the output signal significantly. DR is here defined as the ratio of maximum-to-minimum input photocurrent which can still be sensed by TIA. And DR is mainly determined by the feedback loop of the TIA.

However, the feedback loop also affects the transimpedance gain and the bandwidth of TIA. The improvements of these demands may be contradictory. Therefore, a trade-off should be taken into account among them. In order to protect the TIA from saturation and improve the input current overdrive capability, the full input photocurrent range is divided into two regions to improve the dynamic range [2]. Moreover, the 2-stage compression concept has been described [3]. On the basis of the concept, the full input current range is separated into three regions in this design: inactive, one-active and both-active thus further broadening the DR and increasing the input current overdrive capability.

The sensitivity is defined that the acceptable mean minimum optical power at the specified bit error ratio (BER). And the sensitivity S can be expressed as:

$$S = \frac{Q\sqrt{I_{\text{nin}}}}{R_0} \quad (1)$$

where the Q is the noise distance determined by the signal current and input noise current. For a typical value BER of 10^{-9} in practice, the value of Q is equal to 6. I_{nin} is the total input noise current, and R_0 is the responsivity of the photodetector. For a high speed photodetector, the responsivity is very small (typically 0.04 A/W), which requires more stringent noise performance to obtain high sensitivity [4].

Currently, the work on the TIA presents two trends: one is resolving the bottleneck of the bandwidth, and the other is optimizing the sensitivity and dynamic range [5]. In this design, an

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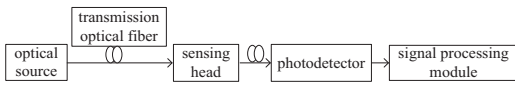


Fig. 1. The block diagram of optical fiber sensing system.

AGC circuit is used to achieve a wide DR. Besides, a shunt transistor is also employed to further enlarge the DR. Based on the previous work [6], the AGC circuit is improved by using peak detector, level shifter, and buffer instead of the MOS transistor and resistor in series. The parallel feedback resistor is replaced by a MOS transistor. So the process variation can be reduced effectively and the dynamic range becomes wider. In order to reduce the signal reflection, output buffer is added in this design. Single to differential circuit is employed to realize the matching of signal output to differential inputs.

2. Circuit implement

The diagram of the whole transimpedance amplifier circuit is shown in Fig. 2. The TIA proposed consists of three-stage cascade push-pull inverter, automatic gain control (AGC), inductive-series peaking, single to differential circuit, and output buffer. The three-stage cascade push-pull inverter is the core of the TIA, and AGC can adjust the gain of the core according to the input signal amplitude. The subsequent block of output will provide a fully differential 50 Ω output driver and reduce the signal reflection.

Three-stage cascade push pull inverter is used to achieve the gain in demand. In order to extend further the bandwidth, the inductive-series peaking technique is used in this design. Fig. 3 shows the circuit structure of three-stage cascade push-pull inverter with inductive-series peaking. Three-stage cascade push-pull inverter is comprised of M_1 – M_9 transistor. The PMOS and NMOS transistors in the push pull inverter can be both biased in saturation region to maximize the transconductance and increase the gain bandwidth product of the entire structure [7]. The voltage drop of the feedback resistor R_f can provide the bias voltage for MOS transistors without an additional bias source and regulate the input matching. The transistor M_3 , M_6 , and M_9 serve as active load so that the amplifier transistors can enlarge their sizes to avoid overshoot. Moreover, it can also increase the bandwidth and minimize the Miller effect. The inductive-series peaking technique is

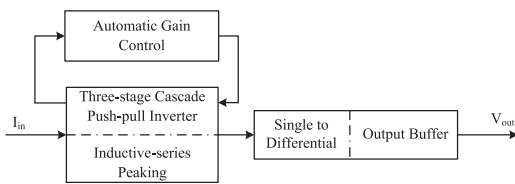


Fig. 2. The overall circuit diagram.

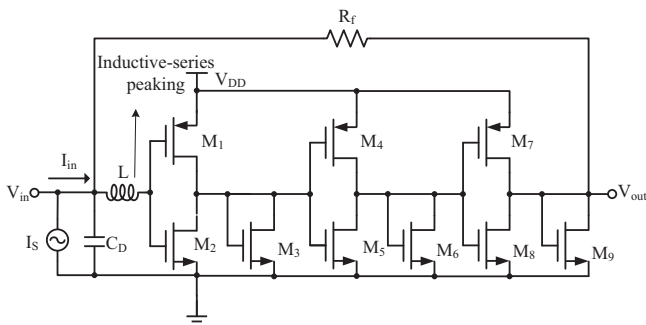


Fig. 3. Three-stage cascade push-pull inverter with inductive-series peaking.

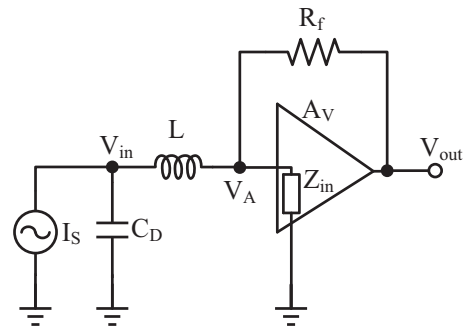


Fig. 4. The simple equivalent model of three-stage cascade push-pull inverter with inductive-series peaking.

realized by the inductor L inserted into the input terminal of three-stage cascade push pull inverter. Compared with the active inductor [8] which normally consists of a MOS transistor and a resistor, the off-chip spiral inductor L used in this design can provide a higher inductance value in the low-voltage high-speed circuits.

The dominant pole of three-stage cascade push pull inverter lies in the input terminal. The transimpedance gain A_R can be expressed as [9]

$$A_R = \frac{V_{out}}{I_{in}} \approx R_f \quad (2)$$

The -3 dB bandwidth without inductive-series peaking can be expressed as [10]

$$f_{-3\text{dB}} = \frac{A_{total}}{2\pi R_f C_{in}} \quad (3)$$

where C_{in} is the input capacitance of three-stage cascade push pull inverter. A_{total} is the total voltage gain.

$$A_{total} = A_{V1} \times A_{V2} \times A_{V3} \quad (4)$$

where A_{V1} , A_{V2} , A_{V3} are respectively the voltage gain of the first stage, the second stage and the third stage push pull inverter.

Fig. 4 is the simple equivalent model of Fig. 3. V_A and Z_{in} are respectively the input voltage and impedance of three-stage cascade push pull inverter.

According to Kirchhoff's current law

$$\frac{V_A - V_{out}}{R_f} + \frac{V_A}{Z_{in}} = \frac{V_{in} - V_A}{Z_L} \quad (5)$$

$$\frac{V_{in} - V_A}{Z_L} + \frac{V_{in}}{1/sC_D} = I_S \quad (6)$$

$$V_{out} = A_{total} V_A \quad (7)$$

where Z_L is the impedance of inductor L . The transimpedance can be expressed as

$$Z_R = \left| \frac{V_{out}}{I_{in}} \right| = \left| \frac{A_{total} R_f}{(1 + sC_D Z_L) \left[1 - A_{total} + R_f \left(\frac{1}{Z_{in}} + \frac{sC_D}{1 + sC_D Z_L} \right) \right]} \right| \quad (8)$$

Bring $Z_{in} = 1/sC_{in}$ and $Z_L = Ls$ into the above equation, then

$$Z_R = \left| \frac{A_{total} R_f}{(1 + s^2 C_D L)(1 - A_{total} + sC_{in} R_f) + sC_D R_f} \right| \quad (9)$$

Assuming that

$$\alpha = 1 + s^2 C_D L \quad (10)$$

Then

$$Z_R = \left| \frac{A_{total}R_f}{\alpha(1 - A_{total} + sC_{in}R_f) + sC_D R_f} \right|$$

$$= \left| \frac{1}{\alpha} \right| \left| \frac{A_{total}R_f}{1 - A_{total} + s(C_{in} + \frac{C_D}{\alpha})R_f} \right| \quad (11)$$

Since $s^2 < 0$, when $\alpha < -1$, so

$$\left| C_{in} + \frac{C_D}{\alpha} \right| < |C_{in} + C_D| \quad (12)$$

At the time, the -3 dB bandwidth with inductive-series peaking can be expressed as

$$f_{-3 \text{ dB}} = \frac{A_{total}}{2\pi (C_{in} + \frac{C_D}{\alpha}) R_f} \quad (13)$$

Comparing Eq. (13) with Eq. (3), we can see that inductive-series peaking can reduce the effect of the photodetector parasitic capacitances C_D on the dominant pole thus extending the bandwidth.

Automatic gain control (AGC) circuit is used to realize wide dynamic range. The structure of AGC circuit is shown in Fig. 5. Comparing to the previous work, the AGC circuit is improved by using peak detector, level shifter, and buffer instead of the MOS transistor and resistor in series. The parallel feedback resistor is replaced by a MOS transistor. So the process variation can be reduced effectively and the dynamic range becomes wider. AGC circuit is made up of two parts (Part A and Part B). In part A, the current source, M_{12} , and R_3 constitute peak detector. The capacitance C_1 is used to store charge. M_{13} and R_4 form level shifter. M_{14} and M_{15} compose buffer. M_{10} takes the place of feedback resistor. The resistance value of the transistor M_{10} will vary with the different control voltage thus

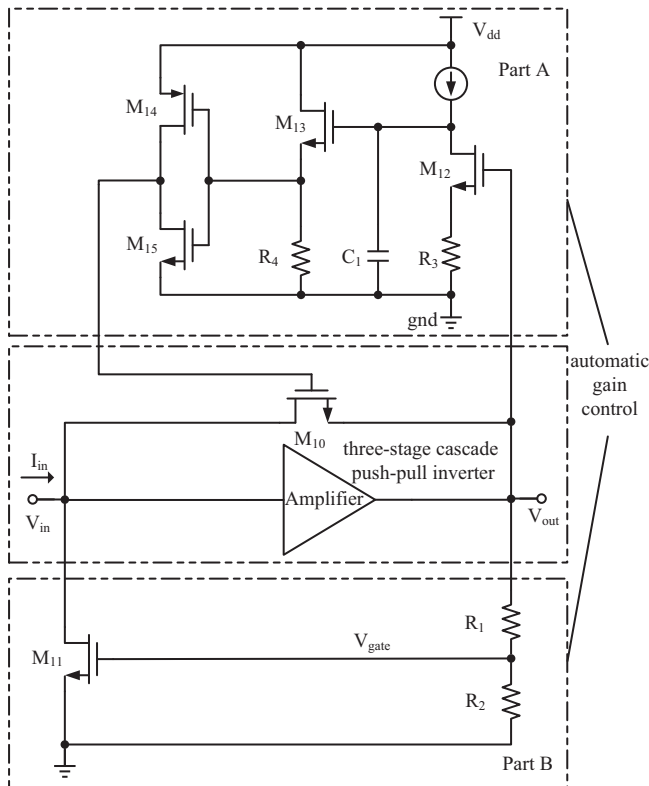


Fig. 5. Automatic gain control circuit.

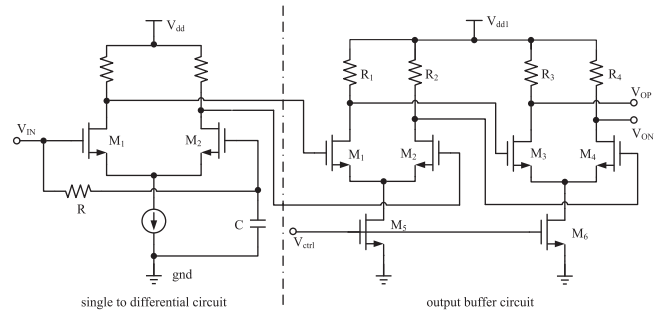


Fig. 6. Output buffer with signal to differential circuit.

adjusting the transimpedance gain. In part B, transistor M_{11} acts as a shunt transistor and forms a parallel current path. When transistor M_{11} is on, a part of photocurrent will flow into ground through M_{11} thus further enhancing the dynamic range. The resistances R_1 and R_2 are regarded as resistive divider.

The full input current range is divided into three regions which includes inactive, one-active and both-active. In the inactive region, the input current is very small and transistors M_{11} and M_{12} are turned off, the transimpedance gain is approximated to the resistance value of M_{10} . The TIA responds linearly to the input current. In the one-active region where the input current has a medium value, the transistor M_{12} starts to be turned on while M_{11} is still off, the transimpedance gain is adjusted by the gate voltage of M_{10} . While in the both-active region, the input current is large enough, so both transistors M_{11} and M_{12} must be turned on, and the transimpedance gain is reduced more seriously which can not be simply calculated.

In order to reduce the signal reflection, output buffer is added in this design. Due to that three-stage cascade push-pull inverter has signal output and output buffer possesses differential inputs, so single to differential circuit must be employed in the design to realize the matching. Fig. 6 demonstrates the structure of output buffer with single to differential circuit. Single to differential circuit consists of common-source differential tubes and RC passive high-pass filter. When the current flowing through the components is direct current, the state of capacitance C is equivalent to open circuit. At the time there is no static current through M_1 and M_2 , so their direct current biases are equal. At high frequency, the state of capacitance C is equivalent to short circuit. Then single to differential circuit outputs differential signals to the subsequent output buffer, which is made up of two-stage cascade differential amplifiers to improve the drive capability. The resistance value of R_3 and R_4 can be set 50Ω to achieve the matching of internal circuit with transmission lines.

3. Simulation results

The TIA proposed is simulated with Cadence-Spectre in SMIC $0.18 \mu\text{m}$ 1P6M CMOS technology. The power dissipation is about 8.1 mW with a 1.8 V supply voltage.

Fig. 7 shows the transimpedance gain versus frequency response of the TIA. From the simulation result of the AC analysis, the bandwidth is about 1.4 GHz and transimpedance gain is up to $87.8 \text{ dB}\Omega$, which is high enough to amplify the receiving photocurrent. When the loop gain equals 1, the gain crossover point is about at the -3 dB bandwidth frequency point on the wave of closed-loop gain namely the transimpedance gain. So for the TIA circuit, the phase margin is about 60 .

Fig. 8 shows the transient response for the output voltage versus input current at different process corners. The input current pulse is the same, of which the pulse-width is 400 ps with a rise/fall time of

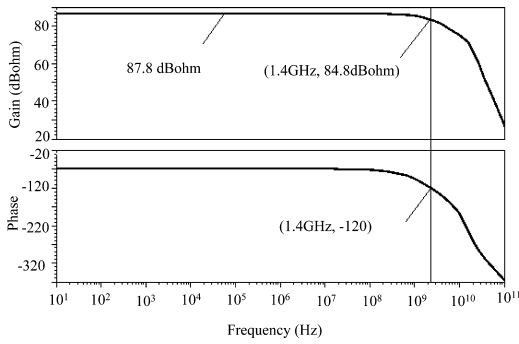


Fig. 7. The transimpedance gain versus frequency response of the TIA.

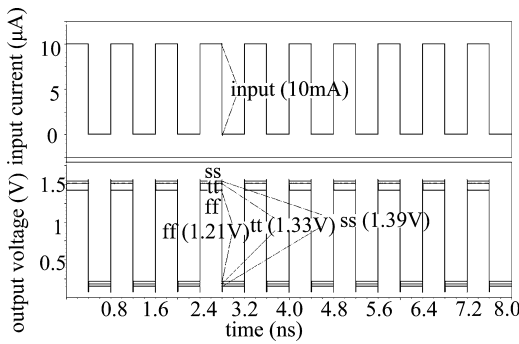


Fig. 8. The transient response for the output voltage versus input current at different process corners.

10 ps and the peak-to-peak current is 10 mA. The simulation result exhibits that the TIA can both respond normally to a fast and large input current. In addition, the output swing of the proposed TIA shows little change at different process corners.

DC-transfer characteristic of the TIA is depicted in Fig. 9. The dynamic range of input current is from 10 nA to 15 mA, which is wider than that of the previous design circuit [5]. As the analysis of the input current referred in section 2, the full range is divided into three regions. The inactive region is from 10 nA (node n_0) to 0.28 mA (node n_1) in which the output voltage increases linearly with the input current. And the one-active region varies from 0.28 mA (node n_1) to 0.76 mA (node n_2) where the output voltage begins to reduce as a result of an attenuated transimpedance gain. The range from 0.76 mA (node n_2) to 15 mA (node n_3) belongs to the both-active region and the output voltage continues to decrease. Moreover, the output voltage does not exceed 1.8 V within the input current dynamic range.

The output noise of the overall circuit is depicted in Fig. 10. As shown in Fig. 10, the maximum output voltage noise is less than

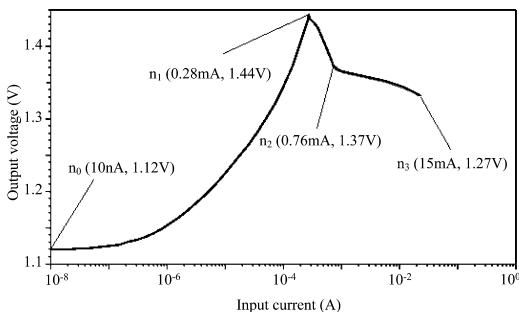


Fig. 9. DC-transfer characteristic of the TIA.

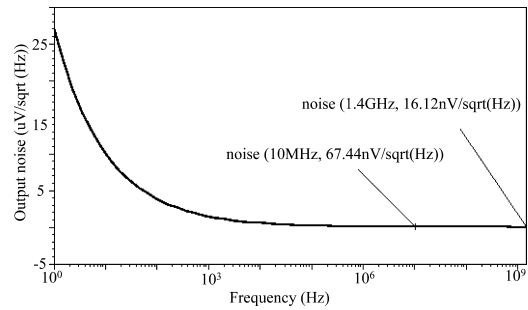


Fig. 10. The output noise of the TIA.

67.4 nV/sqrt(Hz) from 10 MHz to 1.4 GHz. According to the conversion relations of the input equivalent current noise and the output noise, the equivalent input current noise is about 2.75 pA/sqrt(Hz) within the bandwidth. In Eq. (1), the noise distance Q equals 6 for BER of 10^{-9} and the responsivity R_0 is a typical value of 0.04 A/W, the sensitivity S is equal to -6.04 dBm by calculation for the equivalent input current noise of 2.75 pA/sqrt(Hz).

To estimate the effect of the process and mismatch on the proposed TIA, Monte Carlo simulation for the whole circuit is conducted. The result of 200-runs Monte Carlo simulation for the designed TIA is shown in Fig. 11, which is based on cumulative normal probability distribution. Fig. 11(a)–(d) depict the histograms of the output voltage signal when the input current signal I_{in} is equal to 10 nA, 1 μ A, 1 mA, and 15 mA, respectively, where N is the number of Monte Carlo iterations, V_{ideal} is the ideal output voltage without considering the process or mismatch, s_d is the standard deviation, and m_u is the mean value. As one can see, the process and mismatch have little effect on the response of the output voltage signal with the input current signal.

The main performance of this proposed TIA is summarized and compared with some similar works presented in other references in Table 1. The transimpedance gain of this design is 87.8 dB Ω and higher than that of the other related works expect [2]. This effect mainly results from that three-stage cascade push pull inverter is used in the design because the PMOS and NMOS transistors can be

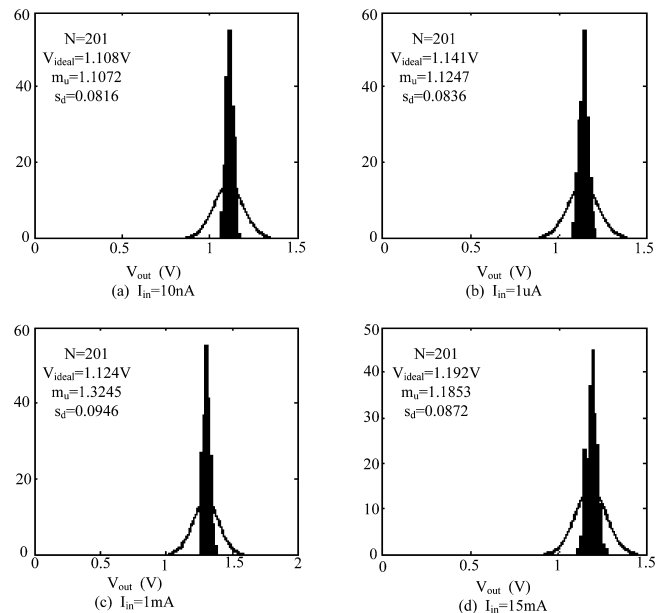


Fig. 11. The histograms of the output voltage signal when (a) $I_{in} = 10$ nA (b) $I_{in} = 1$ μ A (c) $I_{in} = 1$ mA (d) $I_{in} = 15$ mA.

Table 1
Performances summary of the proposed TIA: Comparison with other works.

Reference	Process (CMOS)	Gain (dBΩ)	BW (GHz)	DR	Power (mW)	Noise (rms)
[2]	0.18 μm	97.4	1.6	52.5 dB (3.56 μA–1.5 mA)	6.5 (1.8 V)	Output 18.97 mV
[11]	40 nm	68	0.28	85.2 dB (220 nA–4 mA)	8.7 (1.1 V)	Input 220 nA
[12]	90 nm	85.8	1.4	55 dB (1.77 μA–1 mA)	4.3 (1 V)	Output 2.47 mV
[13]	0.13 μm	82.3	1.8	52 dB (5 μA–2 mA)	118 (N/A)	Input 125 nA
This work	0.18 μm	87.8	1.4	123.5 dB (10 nA–15 mA)	8.1 (1.8 V)	Output 67.4 nV

both biased in their saturation region to maximize the transconductance. The TIA can tolerate an input from 10 nA to 15 mA as the result of the improved AGC circuit in the design. The dynamic range of 123.5 dB is the widest compared to the similar available circuits in those references. Moreover, the power consumption of the TIA is relatively low thanks to the simple three-stage cascade push pull inverter structure.

4. Conclusion

A 0.18 μm CMOS high performance transimpedance amplifier had been presented in this work. It is designed for the optical fiber sensing applications. The TIA can tolerate an input dynamic range of 123.5 dB (10 nA–15 mA) thanks to the improved AGC circuit in the design which makes it come true that the process variation is reduced effectively. The TIA proposed displays a higher transimpedance gain of 87.8 dBΩ with –3 dB bandwidth of 1.4 GHz due to the inductive-series peaking technique. The total power consumption is only about 8.1 mW with a 1.8 V supply voltage due to the simple structure. The maximum rms output noise is less than 67.4 nV/sqrt(Hz) within the –3 dB bandwidth. Therefore, this TIA designed in this paper is perfectly suitable for the optical fiber sensing system.

Acknowledgments

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