A Voltage Independent Islanding Detection Method and Low Voltage Ride Through of a Two-Stage PV Inverter

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***Abstract* -- This paper presents an islanding detection method for a two stage PV inverter. The novelty in this method is that it doesn't rely on instantaneous value of the grid voltage for identifying the islanded condition. Instead, the islanding condition is detected by the saturation of the PI controller of the outer voltage control loop. This makes the proposed detection algorithm more reliable compared to other voltage based detection algorithms, as it is immune to malfunctions caused by the sudden load changes or other transients. In addition, a simple but accurate implementation strategy for low voltage ride through (LVRT) operation is also proposed and integrated with the anti-islanding operation. Both these methods are placed inside the overall control structure that can perform seamless transition between grid-connected and stand-alone modes of operation. The simulation results demonstrate the effectiveness of the proposed anti-islanding and LVRT techniques. Finally, hardware results on a 2 KW laboratory prototype are presented for experimental verification of the proposed anti-islanding and LVRT schemes.**

***Index Terms*-- Islanding, LVRT, Voltage control, Current mode control.**

I. INTRODUCTION

Distributed Generation (DG) and microgrids are getting increased attention day by day for their flexible power controlling capability in renewable energy applications. Photovoltaic (PV) is one of the most popular renewable energy sources. A popular approach for integrating PV panels to the grid is to use a two-stage inverter with a front-end boost (DC/DC) converter followed by an inverter [1].

The basic block diagram of such a system is shown in Fig.1. As can be seen, there are two breakers, one on the load side and the other on the utility supply side. In the event of grid non-availability due to an upstream fault in the power system, it is likely that the utility-side breaker trips under the action of grid-side control. Under such a scenario, the inverter continues to pump power into the local load, resulting in islanding operation [2-3]. Sometimes islanding is desirable, but other times it is not. Islanding can create safety problems

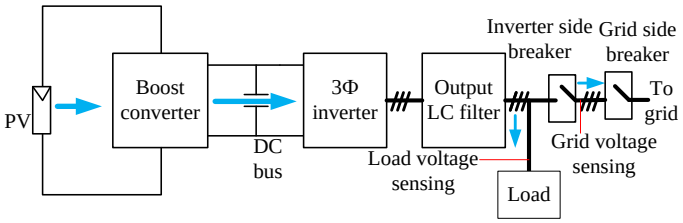

Fig.1: Basic block diagram of the system

for workers and equipments that are not under direct control of the utility. Therefore, islanding condition should be detected, and the inverter should be tripped [4-6]. The inverter side breaker also needs to be opened to isolate the system from the grid. This operating mode of a grid connected inverters is known as anti-islanding.

It is clear that in the event of opening of the grid side breaker following a grid outage, the grid-side voltage sensors start sensing the inverter output voltage. Thus inherent detection of islanding condition is not possible by merely monitoring the grid-side sensors, and specific detection mechanisms are necessary. Sensing signal from grid side breaker is difficult as generally grid side breaker is positioned far away and there also can be many breakers in series. Sensing all signals will also increase cost and complexity of the system. Generally, two approaches are adopted for this purpose. They are classified as - passive methods [1-8] and active methods [2- 9]-[17-19]. Passive methods (like [1], which sense voltage and frequency deviation to observe islanding condition) mostly sense the variation in voltage, frequency or harmonics for islanding detection. Though these methods can detect islanding very fast, they are perceived to be less reliable as malfunction can occur in the event of sudden load change [3]. In active methods, a small amount of reactive power or harmonics is continuously injected into the grid. Islanding is detected by sensing the change in voltage after injection of reactive power or harmonics. In [2], one active method is used where reactive power is injected in steps and frequency variation is observed to determine the islanding condition. Continuously pumping reactive power can affect power factor drastically in low power time. In [3], one method is used which is a combination of frequency dip and phase shift. The continuous change in phase and frequency can give high transient. In [4] and [5] one particular active method is discussed that measures the grid impedance by giving power perturbation. In [6] another method is discussed where small negative sequence current is continuously injected and unbalance in the grid voltage is observed to determine islanding condition. A major drawback of such active methods is their detrimental effect on power quality. Moreover, sometimes a small perturbation of the injected variable into the grid is not enough to produce a significant effect that can be monitored and acted upon. It is not good to supply harmonics and reactive power to the grid.

In this paper, a voltage independent islanding detection method is proposed, where islanding is detected from current saturation of the outer voltage control loop. Once islanding is detected, anti-islanding is done.

In some weak grids, the grid voltage may decrease to a substantially lower voltage compared to the rated grid

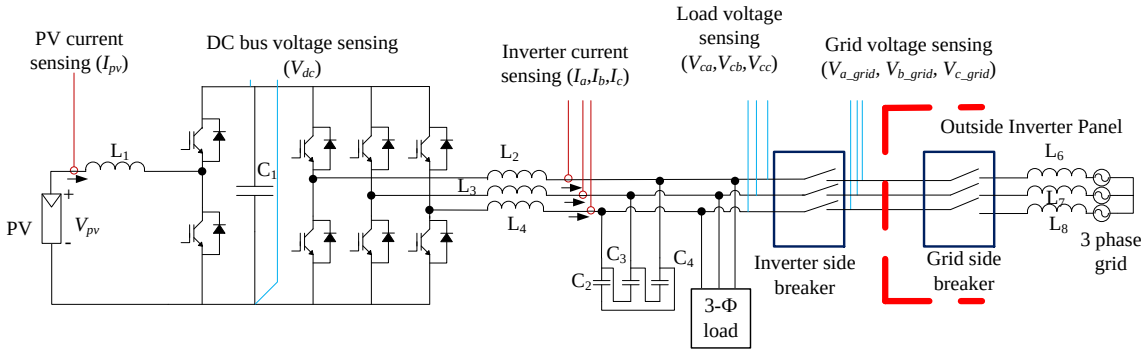

Fig.2: Power circuit diagram of the system

voltage, albeit for a small duration. In this situation, tripping the inverter based on instantaneous value is not a good solution as it would generate unnecessary interruption to the local load. It is better to have a low voltage ride through (LVRT) functionality implemented in the inverter to handle such power system disturbances [10]-[11]. The voltage vs. time curve to be followed during low voltage time is shown in Fig.3 [10],[14]. (One of the widely used curve. It is referred in FGWTR3.) If low voltage occurs for more time than the time specified by the Fig.3, it is considered as grid fault, and inverter should disconnect itself from the grid. Then anti-islanding should be done

An implementation of LVRT method is discussed in this paper. The LVRT method helps the inverter to ride through the low voltage condition if that occurs for a small time. The

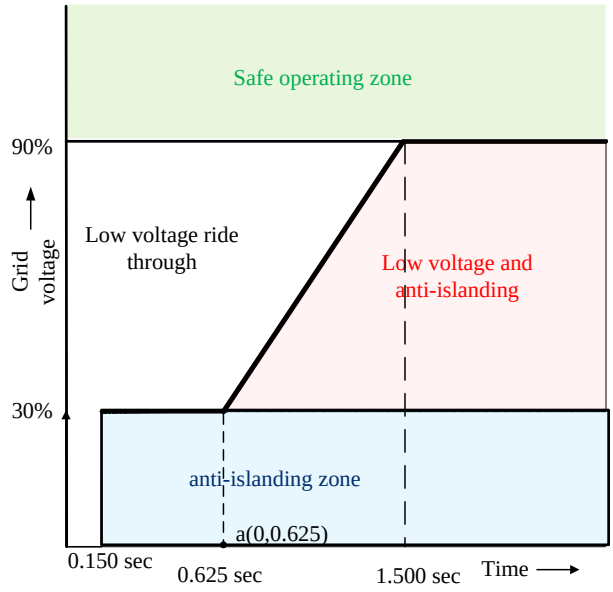

Fig.3: Voltage vs. time curve for LVRT operation

LVRT method leads to anti-islanding if low voltage condition persists for more time than certain time and stand-alone operating mode is not allowed.

The paper has six sections. After the introduction, proposed voltage independent islanding detection method is discussed. Implementation of LVRT method is also discussed in this section. 2nd section also discusses, how islanding detection and LVRT works together to take care of all abnormal grid conditions. Simulation results are provided in the next section. All the algorithms are tested in the laboratory prototype and results are provided in the 4th section. In 5th and 6th sections conclusions and references are provided for detailed understandings.

II. PROPOSED CONTROL TECHNIQUE

The power circuit diagram of a two stage grid connected PV inverter is shown in Fig.2. In normal operating condition, both the breakers remain connected. The grid in this condition works as a power balancing source to the PV inverter. The load voltage remains fixed by the grid.

The control block diagram of the system is shown in Fig.5 [12]. In the grid connected (GC) mode of operation, the inverter side breaker remains connected. As shown in the control block diagram, the DC bus voltage controller gives the d axis current reference of the inverter. The sinθ and cosθ components of the synchronously rotating reference frame are generated by the SRF-PLL [12]. The d and q axis conversions are shown in Fig.4. It is intended that the d axis is aligned to the capacitor voltage vector or V_{cq} is zero. I_q^* is set to zero

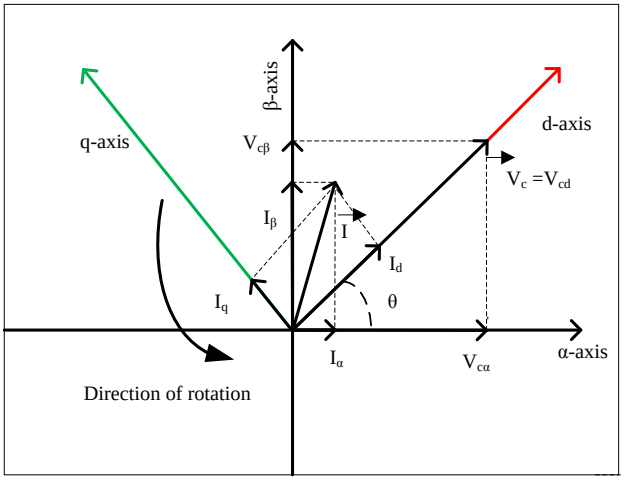

Fig. 4: d and q axis orientation

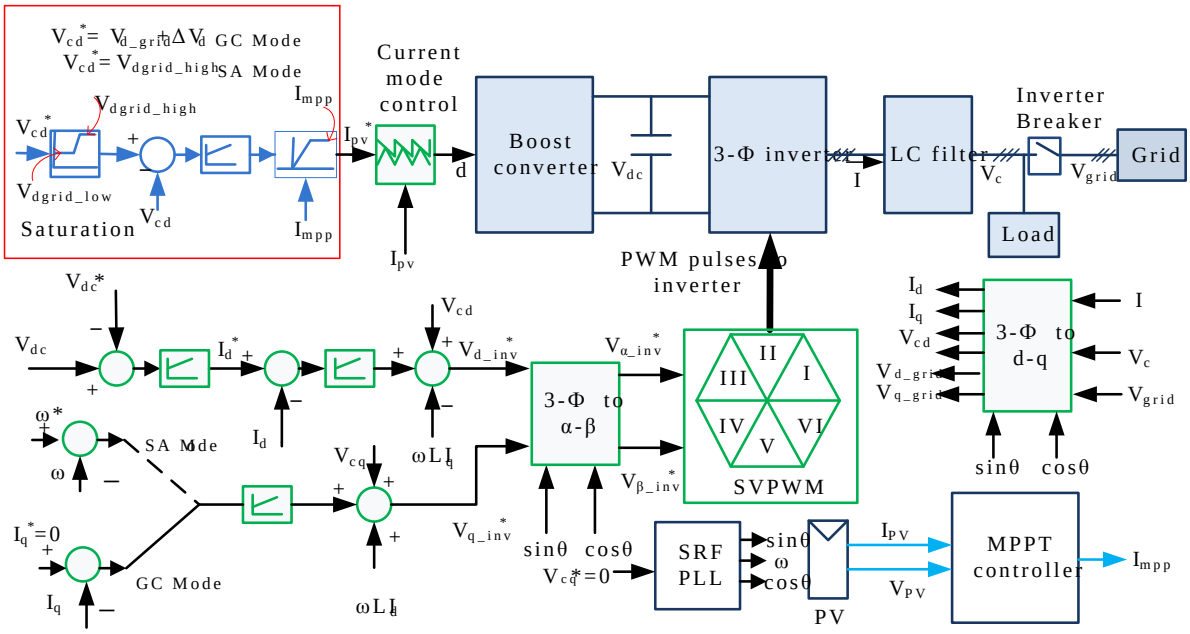

Fig.5: Control block diagram of the two stage PV inverter system with grid connected (GC) or standalone mode (SA) of operation

for unity power factor operation. In GC mode V_{cd} is same as $V_{d\_grid,}$ where V_{d_grid} is the d axis grid voltage. $V_{q\_grid,}$ is zero as it is same as V_{cq} in GC mode of operation. As shown in the block diagram, $V_{cd}^{*} = V_{d\_grid} + \Delta V_d$ is set, where ΔV_d is a small voltage. Now in GC mode, V_{cd} can never reach $V_{d\_grid} + \Delta V_d$ as V_{cd} is same as V_{d_grid}. As a consequence, the reference sends a ΔV_d error to the PI controller of the outer voltage control loop. Eventually the ΔV_d error saturates the PI controller of the outer voltage control loop to its upper limit. The saturation block is shown in the block diagram of Fig.5. The upper limit of the saturation block is the current reference coming from maximum power point tracking (MPPT) controller whereas the lower limit is zero. After outer voltage control loop saturates the boost converter operates with a current reference of I_{mpp}. The control loop and the PLL are same as in [12]. The control structure of Fig.5 can be used for operation in either SA or GC mode and seamless mode transition between them can also be achieved. In this paper, we show that even islanding detection and LVRT can be integrated in the same control structure.

Operation in islanded condition of a grid connected inverter, i.e. in standalone (SA) mode, can create safety problems for the workers in a plant as the inverter may continue to energize some plant load even when grid power supply has failed [13]. Therefore, SA mode of inverter operation may not be allowed and the inverter has to trip. The operation of the system with islanding detection and LVRT is shown in Fig.6. Let's say the system initially is in GC mode. If islanding condition occurs, the system first detects it. After islanding detection, the system goes into SA mode if the operation in islanding mode is allowed. The system trips if the operation in islanding mode is not allowed. When islanding has not occurred, the system continues to check for low voltage condition of the grid. As long as there is no low voltage situation, the system continues to operate in GC mode. When there is a low voltage condition in grid, the system first performs an LVRT test. If the system passes the LVRT test, it continues to operate in GC mode. If the system fails the LVRT test, the system goes into SA mode if islanded operation is allowed. If islanded operation is not allowed, system trips after LVRT test failure. If in SA mode PV does

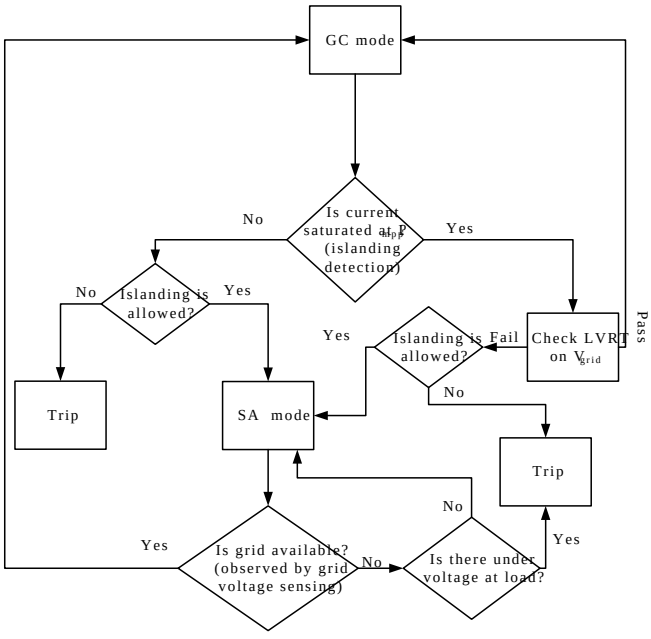

Fig. 6: Operating modes of the system with islanding detection and LVRT

not have enough power to supply the load, low voltage occurs across the load. It is not desirable to operate with low voltage

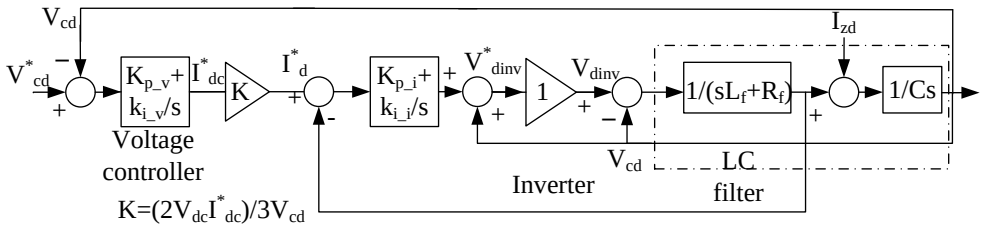

Fig. 7: Control block diagram for the outer voltage control loop design

as it may damage the load. Therefore, in SA mode, if low voltage occurs, the system trips. The islanding detection method and LVRT algorithm are discussed later in this paper.

A. CONTROL LOOP DESIGN

The designs of the all the controllers are discussed here. For design of the inner current control loop, the considered control block diagram is shown in Fig.8. The loop gain of the

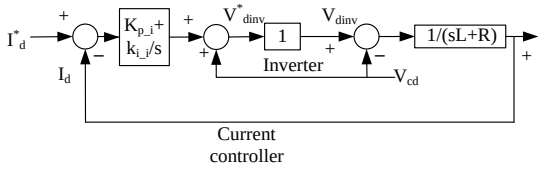

Fig.8: Control loop for design of inner current control loop

control loop is shown in (1).

$$TF = \frac{sK_{p\_i} + K_{i\_i}}{s^2 L + sR} \tag{1}$$

The current control loop is designed for 1kHz bandwidth.

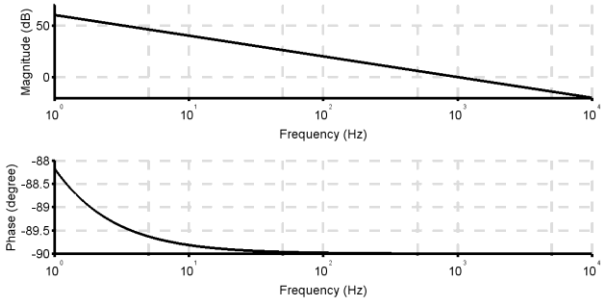

Fig.9: Bode plot of the loop gain of the inner current control loop

(L=2.3mH, R=2mΩ, K_{p_i}=15, K_{i_i}=10). The bode plot of the current control loop is shown in Fig.9. The designed phase margin 90º and gain margin is infinite.

For DC voltage control, the considered control loop is shown in Fig.10. Here current controller transfer function is considered unity as it is very fast compared to DC voltage controller.

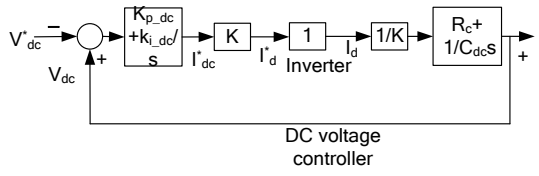

Fig.10: Control loop for design of DC bus voltage controller

The loop gain of the DC bus voltage controller is shown in (2).

$$TF = \frac{(sK_{p\_dc} + K_{i\_dc})(R_c C_{dc} + 1)}{C_{dc} s^2} \tag{2}$$

Here the value of K is shown in (3).

$$K = \frac{2V_{dc} I^*_{dc}}{3V_{cd}} \tag{3}$$

The DC bus voltage controller is designed for 350Hz bandwidth (C=5.6mF, R_c= 20mΩ, K_{p_dc}=0.01, K_{i_dc}=0.1). The designed phase margin is 90º and gain margin is infinite. The bode plot of the DC bus voltage controller is shown in Fig.11.

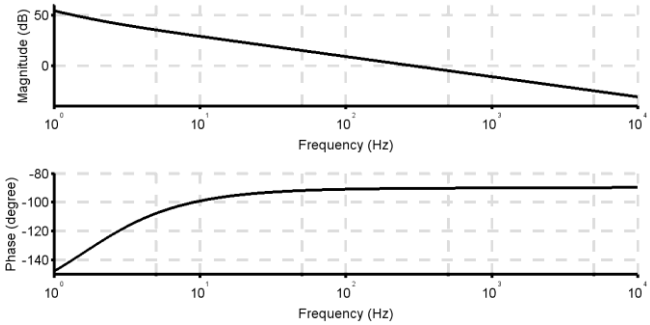

Fig.11: Bode plot of the loop gain of the DC voltage controller.

The control block diagram for outer voltage control loop design is shown in Fig.7. Here The DC current and voltage control loop are not considered as they are very fast compared to the outer voltage control loop. Simplifying Fig. 7 we can get Fig.12.

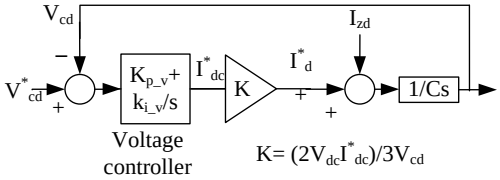

Fig. 12: Simplified control loop for outer voltage controller design

The loop gain of Fig.12 is

$$TF = \frac{K(sK_{p\_v} + K_{i\_v})}{cs^2} \quad (4)$$

K_{p_v} and K_{i_v} are chosen for very low bandwidth (For K=0.098 and C= 30uF the chosen values are K_{p_v}=0.05 and K_{i_v}=5). The chosen values give a BW of 30Hz, phase margin

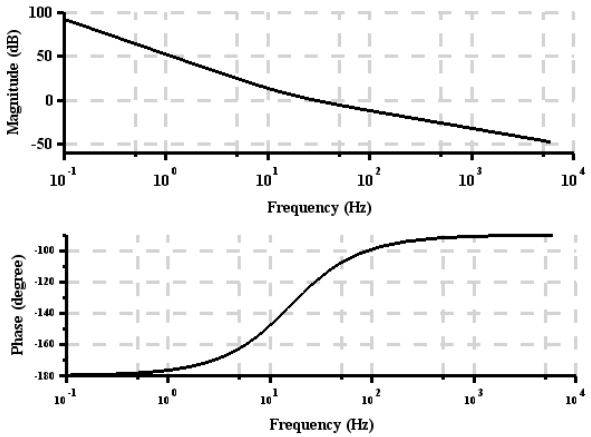

Fig. 13: Bode plot of the loop gain of the outer voltage control loop.

of 60º and gain margin of infinite. The bode plot of the loop gain is shown in Fig.13.

B. ISLANDING DETECTION

The control loop of the inverter is shown in Fig.5. As already discussed, the PI controller of the outer voltage control loop eventually saturates in GC mode. After saturation, the boost converter operates with a current reference of I_{mpp}, that comes from the MPPT controller of PV. In grid connected mode, the system always operates on current control with I_{mpp} as the current reference. Now, in the power system, islanding condition would occur when the grid side breaker gets open (may be due to some upstream fault). The controller of two-stage PV inverter doesn't receive any direct signal from the breaker, as that is not physically at the same location, but the proposed algorithm still detects that islanding has occurred. In this situation, the inverter load terminal voltage is not fixed by the grid anymore. Therefore, the load voltage can now change. Since the grid side breaker during detection remains connected, V_{cd} is same as V_{d_grid}. The command $V_{cd}^* = V_{d\_grid} + \Delta V_d$ tries to increase the load voltage until it reaches V_{dgrid_high}. Assuming that the MPP power is more than the power requirement of the load, (otherwise under voltage happens and LVRT algorithm would operate), the load voltage changes and becomes same as $V_{dgrid\_high,}$. Under this condition the PI controller of the outer voltage control loop comes out of saturation. By monitoring the PI controller coming out of saturation, islanding condition is detected. The control algorithm is shown in Fig.14. If islanding condition occurs anti-islanding (i.e. disconnecting the inverter side breaker and blocking the gate pulses) is done if SA mode is not allowed. After grid becomes available, PLL re-synchronization is done according to [12]. Then the inverter starts with a voltage reference of $V_{d\_grid} + \Delta V_d$ and waits until the PI controller gets saturated. Then it is in the GC mode and islanding detection re-starts.

The proposed islanding detection algorithm requires that, due to the difference between the output power of the PV at MPP and the output power of the inverter, the load voltage has to change to such a steady state value that the PI controller will come out of saturation. Here, we calculate the amount of power that would to be drawn by the grid prior to islanding. With reference to Fig.5, V_{dgrid_high} , is generally specified as 1.1pu. Now, under MPP condition of PV, and prior to islanding, the power balance condition is

$$P_{mpp} = P_{load\_I} + P_{grid} \quad (2)$$

Where, P_{mpp} is the MPP power of PV. P_{load_I} is the power consumed by the load and P_{grid} is the power that is delivered to the grid. Now considering the case that the local load is purely resistive (R) and the grid voltage is at V_{rated} , we have

$$P_{load\_I} = \frac{V_{rated}^2}{R} \quad (3).$$

Where, V_{rated} is the rated load voltage. Now, after islanding, but before the detection, the same amount of PV power would be delivered entirely to the load and the load voltage would rise. Under boundary condition it will be $1.1V_{rated}$. Then,

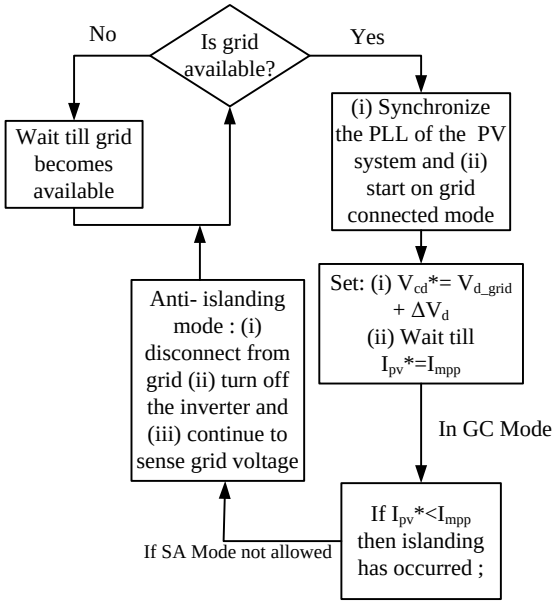

Fig. 14: Islanding detection algorithm

$$P_{load\_F} = \frac{(1.1V_{rated})^2}{R} = 1.21P_{load\_I}$$

Or, $P_{load\_I} + P_{grid} = 1.21P_{load\_I}$ (4)

At boundary condition $P_{grid} = 0.21P_{load\_I}$

$$\frac{P_{grid}}{P_{mpp}} = \frac{0.21P_{load\_I}}{1.21P_{load\_I}} = 17.36\% \quad (5)$$

From (5) it can be said that for islanding detection, the power (P_{grid}) that the grid has to draw prior to islanding should be at least 17.36% of the PV MPP power. If the load is R-L type then that requirement would be even less due to the inductive

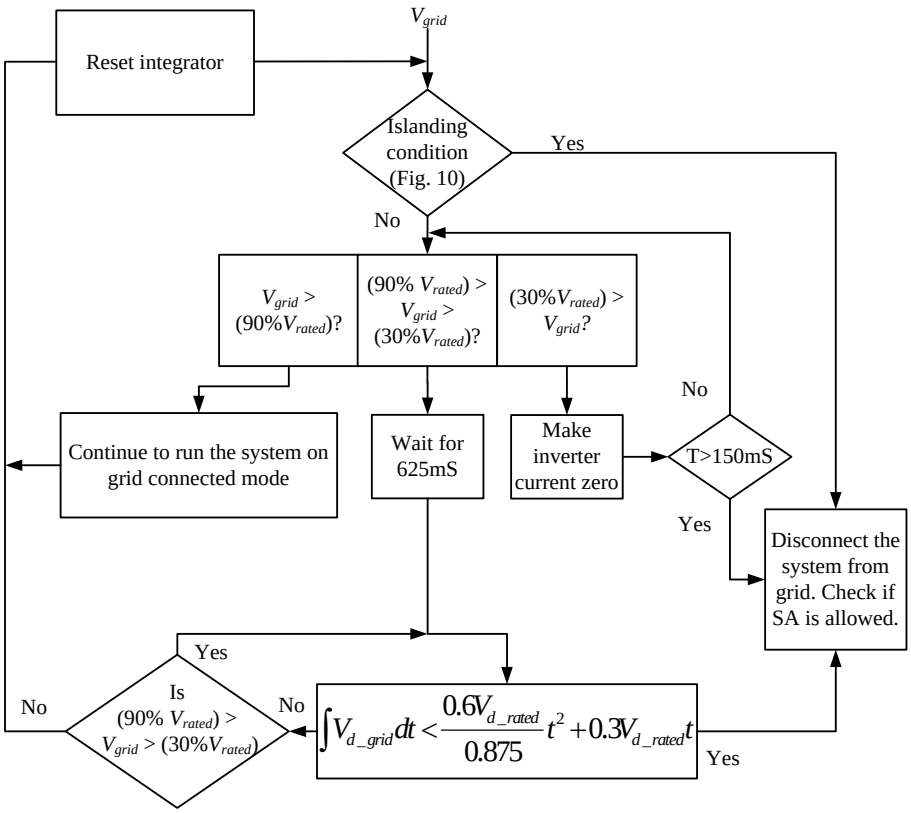

Fig. 15: Implementation logic for LVRT

voltage drop. If the PV power (MPP) is less than the load power prior to islanding then the grid needs to supply at least 19% of the load power for islanding detection to occur, because anti-islanding will be enacted below 90% of the rated grid voltage by the low voltage ride through algorithm as described below. The advantage of the proposed islanding detection method is that it is insensitive to disturbances; because the islanding condition is identified from the de-saturation of the voltage error amplifier comprising of an integrator.

C. LOW VOLTAGE RIDE THROUGH

In a weak utility grid the grid voltage may become low for some amount of time, but it may then recover back to its rated value. In order to maintain the connection of the PV inverter to the grid in this situation, anti-islanding should not be enacted as soon as grid voltage falls below V_{grid_low} , rather the duration also has to be taken into consideration. Fig.4 shows voltage vs. time curve that has to be used as a guideline for determining low voltage condition in the grid. In LVRT algorithm, responds to the grid condition in the following manner: (i) if the grid voltage is below 30% of the rated grid voltage, it has to check that the situation exists continuously for at least 150mS in order to activate anti-islanding steps; otherwise it remains in the grid connected mode, (ii) if the grid voltage is above 90% of the rated grid voltage, the system would continue to run in the grid connected mode and (iii) if the grid voltage is in between 30% and 90% of the rated grid voltage, it has to find out from the curve the allowable time and determine its operation in this region. For finding the allowable time let us shift the origin to point a (0, 0.625 Sec). From this point, the equation of the curve can be written as (6).

$$V_{d\_grid} = \frac{0.6V_{d\_rated}}{0.875}t + 0.3V_{d\_rated} \tag{6}$$

This implies continuous average of grid voltage as in (7),

$$\frac{1}{t}\int V_{d\_grid}(t)dt = \frac{0.6V_{d\_rated}}{0.875}t + 0.3V_{d\_rated} \tag{7}$$

From equation (7) the inequality condition of (8) is obtained,

$$\int V_{d\_grid}(t)dt < \frac{0.6V_{d\_rated}}{0.875}t^2 + 0.3V_{d\_rated}t \tag{8}$$

If at any instant (8) is satisfied, system is disconnected from the grid. The shift of the origin is implemented by giving a computational delay of 625mS from the instant grid voltage becomes low.

The flow chart of the LVRT algorithm is shown in Fig.15. Note that V_{d_rated} is the rated grid voltage and V_{d_grid} is the present grid voltage. As shown in the figure, the system first checks for islanding condition. If islanding has occurred, the system disconnects from the grid. If islanding has not occurred, the system checks for low voltage. If the grid voltage is more than 90% of rated grid voltage, the system continues to operate in GC mode. If the grid voltage is less

than 30% of rated grid voltage, the system waits for 150mS then does anti-islanding. If the grid voltage is in-betweens 30% and 90% of rated grid voltage, system first waits for 0.625Sec. After 0.625Sec system checks for the condition given by

$$\int V_{d\_grid}\,dt < \frac{0.6V_{d\_rated}}{0.875}t^2 + 0.3V_{d\_rated}t\,.$$

If the condition is not satisfied, the system continues to work in GC mode; else it disconnects from the grid by opening the inverter side breaker and trips if SA mode is not allowed. The system waits till the rated grid voltage becomes available again and then it resynchronizes with the grid.

For the PV inverter a faulty grid situation arises when either islanded condition happens or the sag in the grid voltage occurs. The islanded condition is detected by using the first algorithm (Fig.14). On the other hand, if the voltage falls below the rated grid voltage for more than the stipulated amount of time, LVRT algorithm comes into operation for doing anti-islanding (Fig.15). So, by performing the islanding detection in conjunction with the LVRT method all faulty grid conditions can be addressed by the two-stage PV controller. The LVRT algorithm proposed here is very accurate as it is independent of the nature of the voltage sag. This is because the LVRT specification has been formulated as an inequality condition and this condition can be checked by integration of direct axis component of the instantaneous grid voltage.

III. SIMULATION RESULTS

The proposed islanding detection and LVRT algorithms are verified in simulation. The simulation is done in PLECS. The switching frequency is chosen as 10 kHz, same as in the hardware prototype. In simulation, the test condition is as follows: the load is a three phase 10 Ohm resistance directly connected to the inverter, the PV voltage and current at MPP are 300V and 30A and the grid voltage is 200V (line to line).

For testing the islanding detection algorithm, the system is initially allowed to operate in the GC mode for a small amount of time till the outer voltage control loop reaches saturation. After the PI controller saturation, islanding detection algorithm starts working. Fig.16 shows the simulation result of islanding detection. For creating the islanding condition, the grid side breaker is opened intentionally at 1 Sec (The outer voltage control loop is already saturated). As a consequence, at 1 Sec the grid current becomes zero. The load voltage reaches its saturation value as V_{cd}^* and V_{cd} increase as the available power is more than load power. (The extra power was being supplied to the grid). As a result, the outer voltage control loop comes out of saturation. Due to this I_{pv}* (Fig.5) starts decreasing. Detecting that the current (I_{pv}^*) is out of saturation, islanding is detected. After detection, the inverter side breaker is opened and the inverter is tripped but it keeps on monitoring the grid voltage (anti-islanding).

Fig. 17 shows a situation where PV power is less than load power. Here, PV current at MPP is 10A. So, in GC mode the

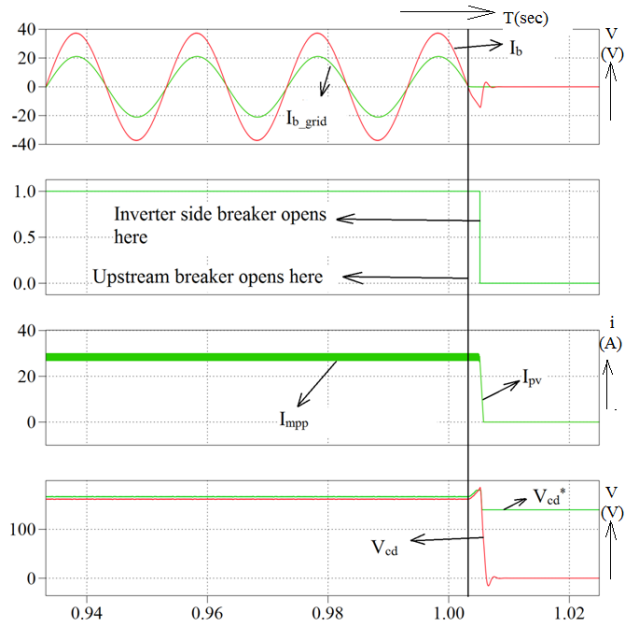

Fig. 16: Islanding detection

grid current is opposite to the inverter current. Here after islanding condition the load voltage falls, as the available power is less than the required load power. Here in this situation anti-islanding is done by the LVRT algorithm. It takes more time (1.3Sec) compared to previous result for

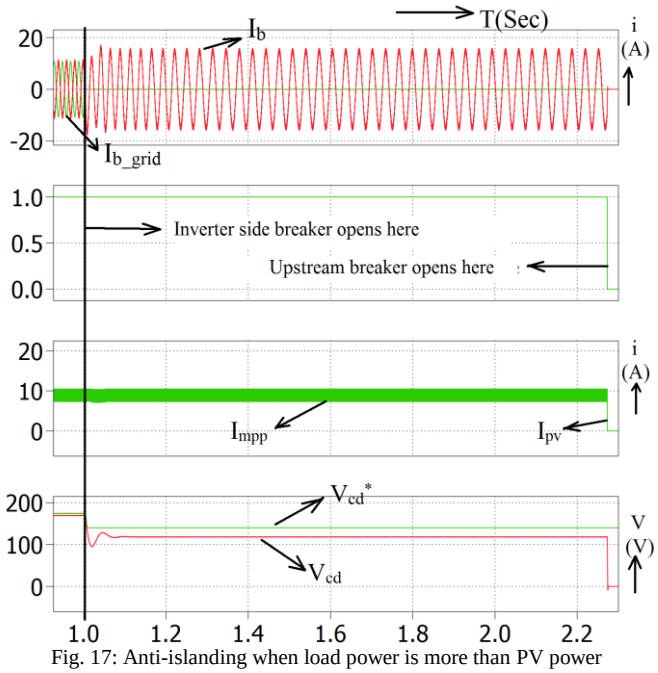

Fig. 17: Anti-islanding when load power is more than PV power

activating anti-islanding steps but the time is less than 2 Sec. So, it still follows IEEE1547[16].

Fig.18-21 shows the simulation results of LVRT. Fig.18 shows the simulation results of LVRT operation where low voltage occurs for a small time (less time than allowable time). As shown in Fig.18 the grid voltage decrease till 1.3 Sec and then it goes back to its rated value. Here low voltage occurs for nearly 1Sec, which is less than the allowable time

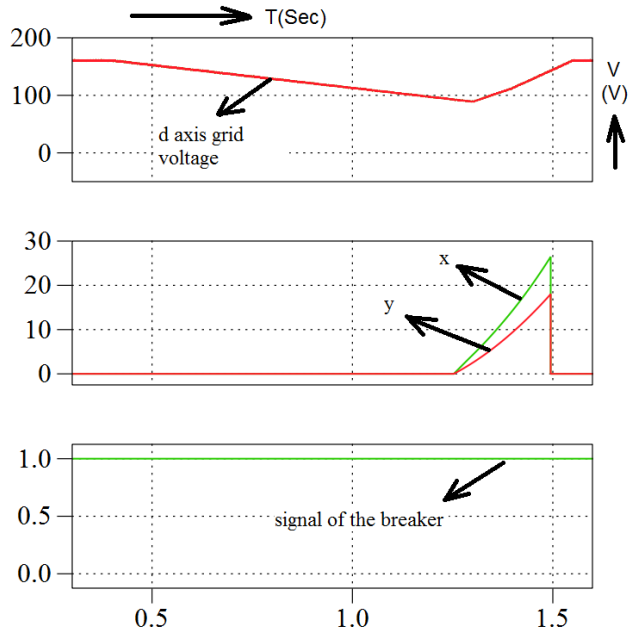

Fig. 18: LVRT operation when low voltage occurs for less time than allowable time

in that condition. Hence, the system rides through the low voltage. The system continues to operate in the grid connected mode as before. The signal to keep the inverter side breaker energized remains high and, the system remains connected to the grid. Here x= $\int V_{d\_grid}\,dt$

and y= $\frac{0.6V_{d\_rated}}{0.875}t^2 + 0.3V_{d\_rated}t$.

Here as soon as grid voltage becomes more than 0.9p.u., the x and y calculation is reseted (becomes zero). Hence the system continues to operate normally in grid connected mode.

Fig. 19 shows a situation where low voltage occurs for more time than the allowable time. As a result, system disconnects itself from grid and anti-islanding occurs. It may be seen that after low voltage occurs, system first waits for 625mSec as discussed in Fig.15. After that, the algorithm starts calculating the allowable time (here x and y calculation starts). Note that when x becomes less than y, anti-islanding is done. Then load voltage becomes zero. Here anti-islanding is activated after x becomes less than y. It can be seen from Fig.19 that, when x becomes less than y, breaker signal is becoming low and load voltage is also becoming zero.

Fig.20 shows a situation where grid voltage becomes less than 30% of the rated grid voltage, but for a very small time. It can be seen that the grid voltage is as low as 5% of the rated grid voltage. Still, the system remains connected and continues to operate in GC mode. Fig.21 depicts a situation where grid voltage becomes less than 30% and it lasts for more than 150mSec duration. Here the system remains

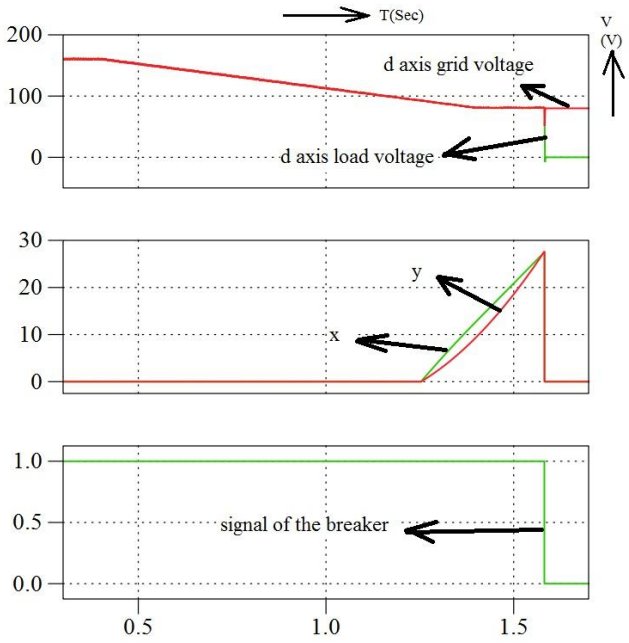

Fig. 19: LVRT operation when low voltage occurs for more time than allowable time

connected to grid till 150mSec and then it gets disconnected. It may be noted that the system does not have to wait for 625mSec. So, the calculation of x and y are not started.

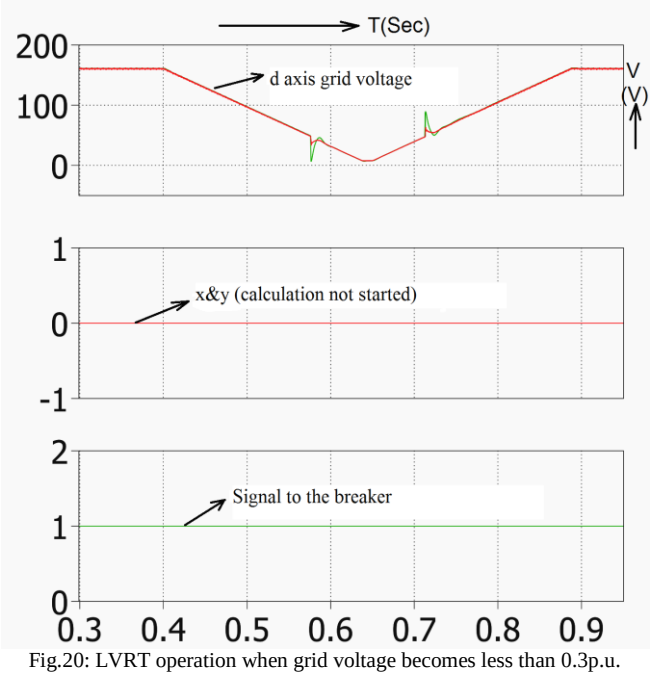

Fig.20: LVRT operation when grid voltage becomes less than 0.3p.u.

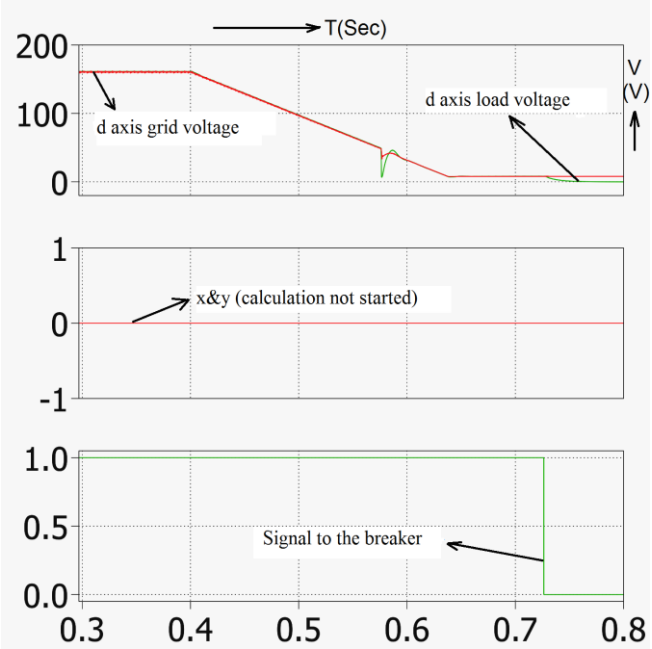

Fig. 21: LVRT operation when grid voltage becomes less than 0.3p.u for

IV. EXPERIMENTAL RESULTS

The proposed control algorithm for islanding detection and LVRT are tested in a 2kW laboratory prototype. The experimental setup consists of one boost converter and one 3 phase inverter. A variable 3 phase resistive load is directly connected to the inverter. The control algorithm is implemented using TMS320F2812 digital signal processor. The switching frequency is 10 kHz. The sampling frequency is same as the switching frequency.

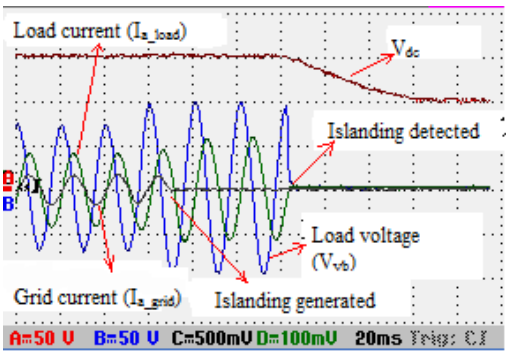

Fig. 22: Islanding detection and anti-islanding (current scale 100mV/A)

Fig.22 shows the experimental result that indicates islanding detection. Islanding condition is created by deliberately opening the grid side breaker without passing that information to the controller. At that instant the grid current becomes zero. After small time (as shown in Fig.22, 60mS), islanding is detected and anti-islanding is done. The islanding detection time is less than 2Sec which satisfies IEEE1547 requirement. As a result, load voltage and load current (directly connected) become zero. After anti-islanding, DC bus voltage falls with a first order response to the level of PV voltage because a resistance is connected across each DC bus capacitor (for balancing the bus voltage).

Fig.23 to Fig.25 show the experimental results of LVRT operation. Here low voltage condition is created by using an autotransformer. (The auto transformer is connected in series between grid and inverter.) Fig.23 shows a situation where low voltage occurs for less duration than allowable time i.e. for about 600msec. It can be seen that the system rides through the low voltage and continues to operate in the GC mode. The power output of the PV at MPP is constant. We know DC power is same as $\sqrt{3}V^*I$ (for unity power factor) which is constant here. As V decreases, I increases to keep the power delivered to the grid constant.

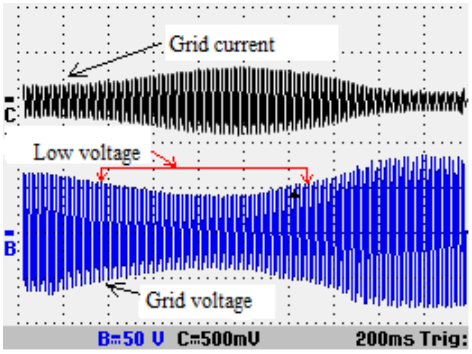

Fig. 23: LVRT operation where low voltage occurs for 600msec. (current scale 100mV/A)

Fig.24 shows a situation where low voltage occurs for more duration than allowable time. (In GC mode load voltage is same as grid voltage). It may be seen that after low voltage occurs, the system waits for 625mSec. Then the calculation of x and y starts. In the experimental set-up these values are

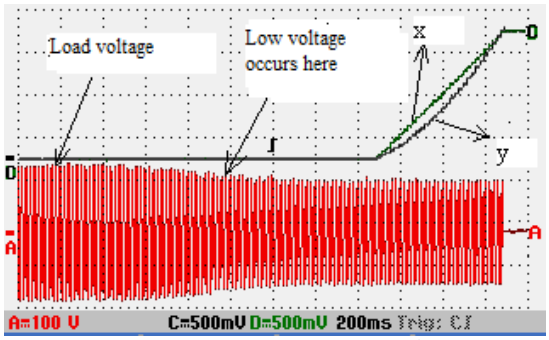

Fig. 24: LVRT operation when low voltage occurs for more time than allowable time

outputted through a DAC (Digital to Analog Converter). Here, as already defined, x= $\int V_{d\_grid}\,dt$

and y= $\frac{0.6V_{d\_rated}}{0.875}t^2 + 0.3V_{d\_rated}t$.

When y becomes more than x, anti-islanding is enacted at that moment. As a result, the load voltage becomes zero.

Fig.25 shows a situation where grid voltage continues to fall from the rated voltage and at certain time has become even less than 0.3p.u. First, in the controller, a delay

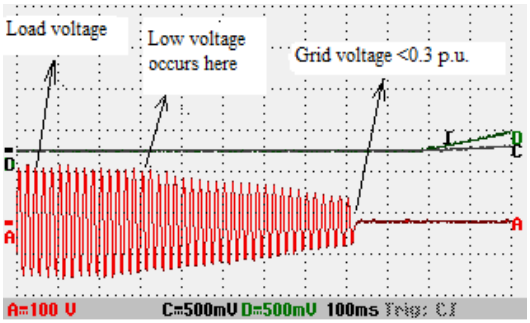

Fig. 25: LVRT operation when grid voltage is less than 0.3p.u.

of 650mSec has started from the instant the voltage has fallen below 0.9p.u. But before it ends another delay of 150mSec gets started from the instant the voltage has fallen below 0.3p.u. In this specific case, the system gets disconnected after this delay, because the grid voltage is still less than 0.3p.u. It can be seen that, 'x & y' calculations have not started at the instant the system trips and would have started had system voltage were between 0.3p.u. and 0.9p.u.

Fig.26 shows the experimental setup that is used to test the prototype. As already discussed the experimental

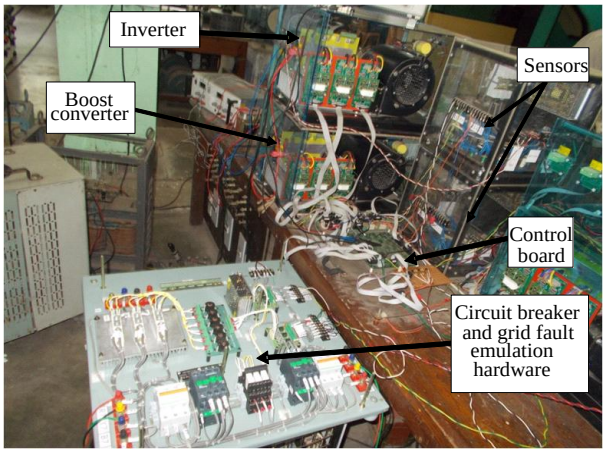

Fig. 26: Experimental test setup

setup consists of a boost converter, an inverter, circuit breakers and voltage and current sensors. A 3 phase variable resistive load is used as a local load. The algorithm is implemented in a control board consist of TI's digital signal processor TMS320F2812.

V. CONCLUSIONS

In this paper an integrated control algorithm for islanding detection and LVRT operation of a two-stage PV inverter is proposed and verified. Islanding is detected from the status of current saturation at the output of the inverter voltage control loop. The advantage of this method is that it is insensitive to disturbances as it does not depend upon the instantaneous value of the grid voltage. The islanding detection time is less than 2 Sec in all cases. It therefore satisfies IEEE1547 standard. The LVRT algorithm proposed here is very accurate as it is independent of the nature of the voltage sag. This is because the LVRT specification has been formulated as an inequality condition and this condition can be checked by integration of direct axis component of the instantaneous grid voltage. The developed control structure is versatile as it can be used for both stand-alone and grid-connected mode of operation with seamless transition of modes in which interactive islanding detection and LVRT features are incorporated along with the MPPT. The algorithm is tested comprehensively in PLECs simulation. The operation of the complete system is tested using a digital platform consisting of DSP TMS320F2812. It is observed that the proposed algorithm ensures fast islanding detection and provides a reliable low voltage ride through performance.

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