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Analytical Design of Passive *LCL* Filter for Three-phase Two-level Power Factor Correction Rectifiers

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***Abstract*— This paper proposes a comprehensive analytical *LCL* filter design method for three-phase two-level power factor correction rectifiers (PFCs). The high frequency converter current ripple generates the high frequency current harmonics that need to be attenuated with respect to the grid standards. Studying the high frequency current of each element proposes a non-iterative solution for designing an *LCL* filter. In this paper, the converter current ripple is thoroughly analyzed to generalize the current ripple behavior and find the maximum current ripple for sinusoidal PWM and third-harmonic injection PWM. Consequently, the current ripple is used to accurately determine the required filter capacitance based on the maximum charge of the filter capacitor. To choose the grid-side inductance, two methods are investigated. First method uses the structure of the damping to express the grid-side filter inductance as a function of the converter current ripple. Reducing the power loss in the filter and optimizing the grid-side filter inductance is the main focus of the second method which is achieved by employing line impedance stabilization network (LISN). Accordingly, two *LCL* filters are designed for a 5 kW silicon-carbide (SiC) based three-phase PFC. Various experimental scenarios are performed to verify the filters attenuation and performance.**

***Index Terms*— AC-DC power conversion, Passive filters, Power filters, Pulse width modulated power converters.**

NOMENCLATURE

Δi	Converter current ripple
$\Delta i_{g,max}$	The maximum allowed grid current
Δi_{peak}	Peak of the converter current ripple
ΔV_{ripple}	AC voltage ripple of filter capacitor
ω_g	Fundamental angular frequency of the grid
ω_h	h^{th} angular frequency of the grid
$C_{d,min}$, $C_{d,max}$	Minimum and maximum damping filter capacitance
C_f	Filter capacitance
f_{res}	Resonant frequency of the filter
f_{sw}	Switching frequency
i	Instantaneous converter current
i_C	Instantaneous filter shunt branch current
i_g	Instantaneous grid current
LISN	Line impedance stabilization network
L_c	Converter-side inductance
L_f	Grid-side filter inductance
L_g	Grid inductance
m_3	Modulation index of the 3rd harmonic
m_a	Modulation index
PCC	Point of common coupling
R_{LISN}	LISN resistance
S	Apparent power
T_{sw}	Switching period
v_{an}	Converter voltage
V_b	Base voltage
v_c	Instantons filter shunt branch voltage
V_{dc}	DC link voltage
v_{Lc}	The converter-side inductor voltage
v_{Lf}	The grid-side inductor voltage
v_{PCC}, V_m	Instantaneous and peak voltage of the PCC
v_x^*	Reference voltage of phase x
v_{xN}	AC link voltage of phase x
WBG	Wide band gap
Z_b	Base impedance
Z_{grid}	Grid impedance

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I. INTRODUCTION

THESE days, three-phase grid-connected PWM voltage source converters (VSCs) in power factor correction (PFC) applications with two-level or multilevel structure are widely used in many applications [1]-[5]. With the improvement of semiconductor technology, the switching frequency of these converters is increasing. Due to the switching of the converter, high frequency current harmonics are injected to grid and they need to be attenuated complying with the strict grid standards. To attenuate the harmonic contents at high frequencies, relying on the boost inductor of the three-phase VSC leads to a bulky inductor with high power losses and it degrades the dynamic performance of the converter [7]. Employing high order filters such as *LCL* filter to fulfill the grid standards are highly attractive and have been studied in many researches [7]-[22].

The method towards designing *LCL* filter of a converter can be categorized into two general approaches. In the first approach, the converter-side inductor is designed to limit the converter current ripple. Then the rest of the filter parameters are chosen to fulfill the grid standard [7]-[16]. In [7], a general and step-by-step approach for designing an *LCL* filter of grid-

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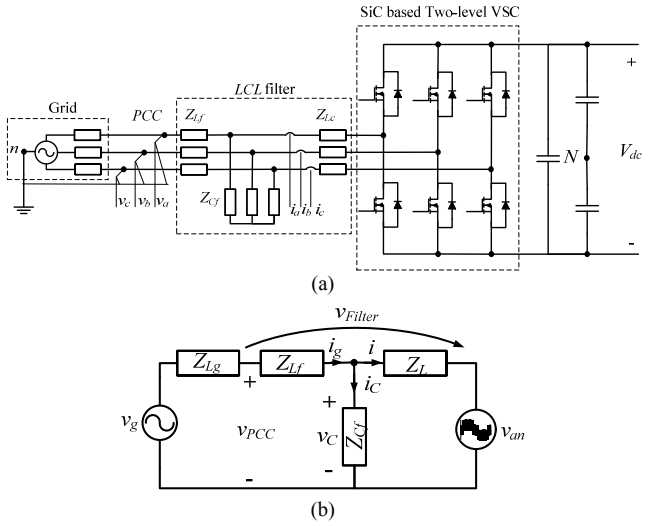

Fig. 1. (a) The schematic of a three-phase two-level PFC and (b) the generic equivalent circuit of the filter.

connected rectifiers has been introduced. In the presented method, the filter parameters are achieved by iteration. The maximum filter capacitance is also defined by the maximum absorbed reactive power. The converter-side inductor selection, however, is not explained in [7]. An attempt to optimize *LCL* filters in terms of loss and size is done in [9]. The minimum required converter-side inductance for space vector modulation (SVM) is derived based on the operating principle of the converter. The filter capacitance is derived as a function of the grid-side inductance. In [10], the maximum current ripple for a three-level SVM neutral point clamped (NPC) grid-connected converter is studied. A margin for combination of the filter capacitance and the converter-side inductance based on total harmonic distortion (THD) is introduced. However, the final values of these two parameters have to be achieved by iteration. The change of the power factor and its impact on the maximum current ripple are also simulated in this paper.

The second approach for designing the filter focuses on calculating a limit for both converter and grid side filter inductances and afterwards chooses the rest [17]-[19]. In [17], despite of an iterative solution for designing *LCL* filter, a margin for the converter and grid side inductances have been calculated for different filter configurations (*L* or *LCL* filter). The filter resonant frequency must be chosen to start calculating the filter parameters. In [18], the grid and converter side inductances are also calculated together. The resonant frequency must be known to start calculating the filter parameters. Therefore, the methods needs iteration to make sure that grid standard is fulfilled.

Damping of the *LCL* resonance can be done by active or passive methods [20]-[27]. Different passive damping methods have been analyzed and compared from different perspectives in researches [20]-[23]. In [20], the dissipated power of different passive damping configurations is investigated and reviewed. The quality factor of the filter as a parameter for finding a proper damping resistor is used in [21].

TABLE I
GENERAL SYSTEM SPECIFICATIONS AND BASE VALUES FOR PER-UNIT

Variable	Description	Value
P_{nom}	Nominal power (kW)	5
V_{ac}	Phase source voltage- rms (V)	230
V_{dc}	DC link voltage (V)	
f_{sw}	Switching frequency (kHz)	45
f_g	Grid frequency (Hz)	50
Z_g	Grid impedance (Ω)	20%×Z_b[1]

[1]The maximum grid impedance has been calculated by maximum short circuit current at PCC using IEEE-519 standard.

Many studies have worked on filter design from different perspectives. Filter parameters are often calculated by iterations. To avoid iteration and achieve an optimized filter, the current and voltage behavior of each filter elements needs to be mathematically analyzed. This paper analytically studies the current and the voltage behavior of the filter from converter to grid. A general expression for high frequency converter current ripple is presented in Section III. Accordingly the minimum and maximum required filter capacitance is also derived. Then, the impact of passive damping on the grid-side inductor is studied and the grid-side inductance is presented as a function of the damping resistor and the converter current ripple. To accurately and optimally define the minimum grid-side filter inductor, line stabilization network (LISN) is used. In Section IV, two *LCL* filters are designed to verify the proposed methods for a 5 kW three-phase PFC and different experiments are performed.

II. SYSTEM DESCRIPTION

In Fig. 1(a), the schematic of a three-phase two-level PFC is shown and the specifications are listed in TABLE I. 1.2 kV, 36 A silicon-carbide (SiC) MOSFETs are utilized for this converter. To fulfill the grid standard, the converter is connected to the grid via a filter. The filter consists of a converter-side inductor (L_c), a grid-side inductor (L_f), and a filter shunt branch (Z_C). The inductances are shown with impedance to include the resistive element of the inductance. The filter shunt branch can be replaced with different combination of passive elements.

The harmonic current injection limit for grid-connected system where the rated voltage at point of common coupling (PCC) is 120 V to 69 kV is recommended by IEEE 519-2014 standard (as listed in TABLE II).

III. FILTER DESIGN

In this section, the filter parameters will analytically be designed and a general method will be presented. For further analysis several assumptions have to be taken as follows:

TABLE II
MAXIMUM CURRENT HARMONIC DISTORTION IN PERCENTAGE OF RATED CURRENT ACCORDING TO IEEE519-2014 [6]

Harmonic order	5	7	11	13	17	19	$23 \leq h < 35$	$35 \leq h \leq 50$
I_h/I_g[*,**](%)	4	4	2	2	1.5	1.5	0.6	0.3

[*]Even harmonics are limited to 25% of the odd harmonics.
[**]I_g: maximum grid current and I_h: h^{th} grid current harmonic.

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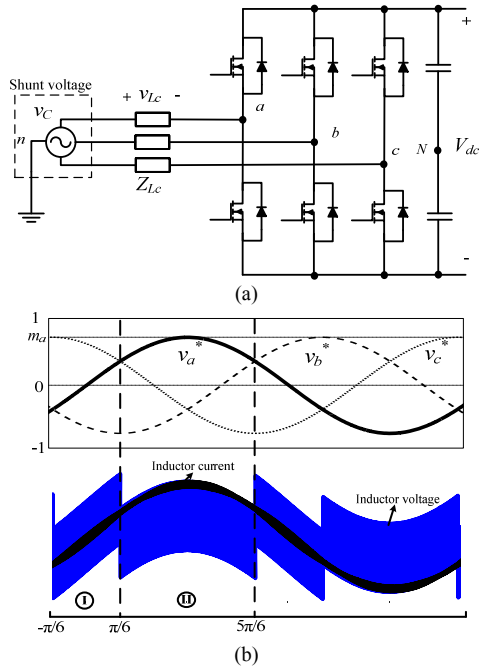

Fig. 2. (a) Simplified schematic of three-phase grid-connected voltage source converter, (b) the inductor current and voltage waveforms.

1) The grid voltage is balance. Therefore, all the analyses are presented for only one phase (e.g. phase '*a*');
2) The switching frequency is much higher than the grid frequency (i.e. $f_{sw} >> f_g$);
3) The modulation is center-based sinusoidal PWM.
4) Unity power factor is assumed.

The equivalent single-phase circuit can be depicted as shown in Fig. 1(b). The filter voltage is found as follows:

$$v_{\text{filter}}(t) = v_{PCC}(t) - v_{an}(t) \tag{1}$$

where v_{filter} is the filter voltage. v_{an} is expressed as a function of the common mode voltage and the ac link voltages.

By analyzing the fast Fourier transform (FFT) of the converter voltage, the largest converter voltage harmonics happen at switching side-band frequency as $f_{sw} \pm 2f_g$ [17],[30].

A. Converter-side inductor

Since minimum required inductance depends on the modulation index, the following analysis is divided into linear and over-modulation.

1) Linear modulation region

If the filter is designed correctly, the voltage after the converter-side inductor (i.e. voltage of the shunt branch v_C) is essentially sinusoidal and the amplitude is close to v_{PCC} (small voltage drop on L_f). Therefore, the converter-side inductor voltage is independent from the filter configuration and the converter voltage determines the minimum required inductance. In this case, the schematic in Fig. 1(a) can be simplified to Fig. 2(a). Consequently, in (1) instead of the filter voltage, the inductor voltage can be replaced. Fig. 2(b) shows the inductor voltage and the resultant inductor current. It indicates that the inductor voltage shows a repetitive pattern in one grid period. There are two time intervals that the inductor voltage has similar behavior. The first interval is when the reference voltage of "phase *a*" is between the other phases (i.e. interval I: $-\pi/6 < \omega_g t \le \pi/6$). The next interval is when the reference voltage of "phase *a*" is larger than the other references (i.e. interval II: $\pi/6 < \omega_g t \le 5\pi/6$).

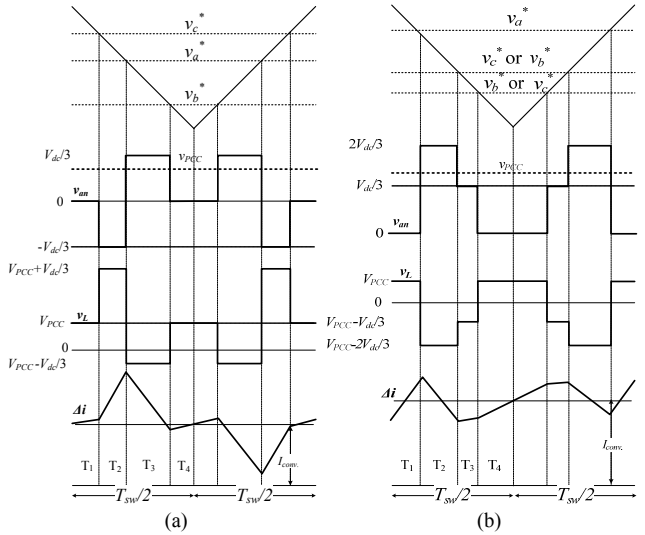

Fig. 3. General behavior of the converter current at (a) time interval I and (b) time interval II ($I_{conv.}$ is the average of the converter current).

The general current ripple behavior in one switching cycle of each time interval is shown in Fig. 3(i.e. time interval I and II in Fig. 2(b)). Using the general equation of an inductor (2), the average square value of the current ripple can be expressed as (3) and (4) for time interval I and II, respectively.

$$\Delta i(t) = \frac{v_c(t) - v_{an}(t)}{L_c}\Delta t \tag{2}$$

In (3), $v = v_a^*/V_{\text{dc}}$, $T_1 = (1\text{-}v_c^*)$, $T_2 = v_{ca}^*$, and $T_3 = v_{ab}^*$ and in (4), $T_1 = (1\text{-}v_a^*)$, $T_2 = v_{ac}^*$ and $T_3 = v_{cb}^*$.

This observation also illustrates that in each time interval, there is a maximum current ripple. For the first time interval, the maximum current ripple occurs at zero crossing (i.e. $\omega_g t = 0$). The voltage references are shown in Fig. 4(a). T_2 and T_3 are equal as well as T_1 and T_4. The maximum current ripple for the second interval occurs at peak current (i.e. $\omega_g t = \pi/2$). The voltage references are shown in Fig. 4(b). The maximum current ripple in each interval is calculated as follows:

$$\Delta i_{peak} = \frac{\sqrt{3}}{12}\frac{V_{dc}}{f_{sw}L_c}m_a \tag{5}$$

$$\left\langle \Delta i^2 \right\rangle = \left(\frac{V_{dc}}{\sqrt{3}L_c}\right)^2 \frac{T_{sw}^2}{32}\left[\frac{(vT_1)^3}{v(3v+1)} - \frac{2\left((v+1/3)T_2 + vT_1\right)^3}{3v^2 - 1/3} + \frac{\left((v-1/3)T_3 + (v+1/3)T_2 + vT_1\right)^3}{v(3v-1)}\right] \quad \text{(I)} \tag{3}$$

$$\left\langle \Delta i^2 \right\rangle = \left(\frac{V_{dc}}{\sqrt{3}L_c}\right)^2 \frac{T_{sw}^2}{32}\left[\frac{(vT_1)^3}{v(3v-2)} - \frac{2\left((v-2/3)T_2 + vT_1\right)^3}{3v^2 - v + 2/3} + \frac{\left((v-1/3)T_3 + (v-2/3)T_2 + vT_1\right)^3}{v(3v-1)}\right] \quad \text{(II)} \tag{4}$$

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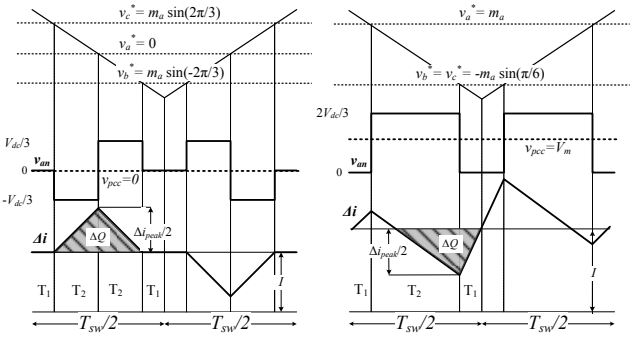

Fig. 4. Converter current ripple at (a) zero crossing and (b) peak current.

$$\Delta i_{peak} = \frac{V_m}{2 f_{sw} L_c}\left(1 - m_a/2\right) \tag{6}$$

Maximum current ripple is at the peak of the current when (7) is correct.

$$\frac{V_{dc}}{V_m} \le \sqrt{3}\left(\frac{2}{m_a} - 1\right) \tag{7}$$

Further simplification of (7) gives that for $m_a \le 0.845$ the maximum current ripple happens at peak of the current.

2) Over-modulation region

From (5) and (6), the inductance value is directly a function of the dc link voltage. By extending the linearity of the modulation, in addition to better dc link usage the inductance can be further reduced. To extend the linearity of modulation, third harmonic injection PWM (THIPWM) is used.

In THIPWM, the reference waveforms become as follows:

$$\begin{cases} v_a^* = m_a \sin \omega_{grid} t + m_3 \sin 3\omega_{grid} t \\ v_b^* = m_a \sin\left(\omega_{grid} t - 2\pi/3\right) + m_3 \sin 3\omega_{grid} t \\ v_c^* = m_a \sin\left(\omega_{grid} t + 2\pi/3\right) + m_3 \sin 3\omega_{grid} t \end{cases} \tag{8}$$

At zero crossing the reference voltage of phase *a*, *b*, and *c* are 0, $m_a\sin(-2\pi/3)$, and $m_a\sin(2\pi/3)$, respectively. It can be seen that the effect of the injected third harmonic does not appear in the resultant reference waveforms and the references are similar to the linear modulation. The only difference here is that the modulation index can be extended to $2/\sqrt{3}$. The reference voltages and the current ripple in one switching cycle are depicted in Fig. 5(a). The time intervals in one switching cycle are equal to one fourth of the switching cycle (the switching dead-time is neglected). Therefore, the current ripple is calculated using the inductor voltage.

$$\begin{cases} \Delta i = \dfrac{V_{dc}/3}{L_c} t \quad 0 < t < T_s/4 \\ \Delta i = -\dfrac{V_{dc}/3}{L_c}\left(t - T_s/4\right) + \dfrac{V_{dc}/3}{L_c} T_s/4 \quad T_s/4 < t < T_s/2 \end{cases} \tag{9}$$

According to the current ripple waveform, the maximum current ripple for $m_a=2/\sqrt{3}$ is found as:

$$\Delta i_{peak} = \frac{V_{dc}}{6 f_{sw} L_c} \tag{10}$$

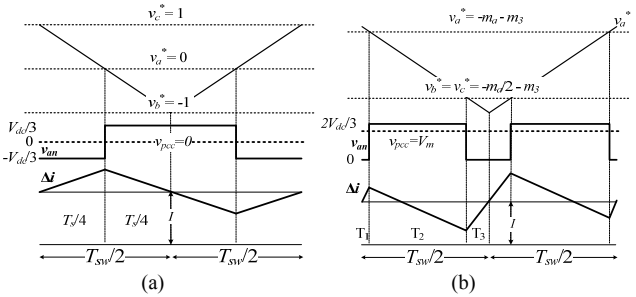

Fig. 5. The current ripple for THIPWM (a) at zero crossing ($m_a = 2/\sqrt{3}$) and (b) at peak of the current.

If in (5) instead of m_a the maximum modulation index in THIPWM or SVM is replaced (i.e. $m_a=2/\sqrt{3}$) then (10) is obtained. Therefore, (5) is the general form of current ripple at zero crossing of a three-phase two-level PFC using continues PWM such as SPWM, THIPWM or SVM.

The same procedure can be done for the peak current and its current ripple for THIPWM. To have a general expression for current ripple at peak current the term m_3 will be kept as it is (it can be set to one-sixth or one-fourth of m_a). The reference voltages are shown in Fig. 5(b).

$$\begin{cases} \Delta i = \dfrac{\sqrt{3} m_a V_{dc}/3}{L_c} t \quad 0 < t < T_1 \\ \Delta i = \dfrac{\sqrt{3} m_a V_{dc}/3 - 2V_{dc}/3}{L_c}\left(t - T_1\right) + \dfrac{\sqrt{3} m_a V_{dc}/3}{L_c} T_1 \quad T_1 < t < T_1 + T_2 \\ \Delta i = \dfrac{\sqrt{3} m_a V_{dc}/3}{L_c}\left(t - T_1 - T_2\right) + \dfrac{\sqrt{3} m_a V_{dc}/3 - 2V_{dc}/3}{L_c} T_2 + \\ \dfrac{\sqrt{3} m_a V_{dc}/3}{L_c} T_1 \quad T_1 + T_2 < t < T_{sw}/2 \end{cases} \tag{11}$$

where time intervals $T_1= (1-m_a+m_3)T_{sw}/4$, $T_2 = 3m_aT_{sw}/8$, and $T_3 = (1-m_a/2-m_3)T_{sw}/4$.

According to (11) and Fig. 5(b), the current ripple for this switching cycle is obtained as follows:

$$\Delta i_{peak} = \frac{\sqrt{3} V_{dc}}{6 L_c f_{sw}} m_a \left(1 - \frac{m_a}{2} - m_3\right) \tag{12}$$

Comparing (10) and (12) demonstrates that the current ripple at the peak current for over-modulation is smaller than the zero-crossing current ripple. This confirms that since in over-modulation m_a is larger than 0.845 then certainly the current ripple at zero crossing is dominant.

B. Filter capacitor

Position of the current and the voltage sensors in PFCs can affect the power factor and the control. With the sensor positions shown in Fig. 1(a), unity power factor cannot be achieved. To minimize the phase difference between the voltage and the current, absorbed reactive power by the filter capacitor is limited to 5% of nominal power [8].

$$\omega_g Z_b C_{f,\max} = 0.05 \tag{13}$$

Assuming that the current ripple flows through the filter capacitor, then the shaded area in Fig. 4 represents a charge

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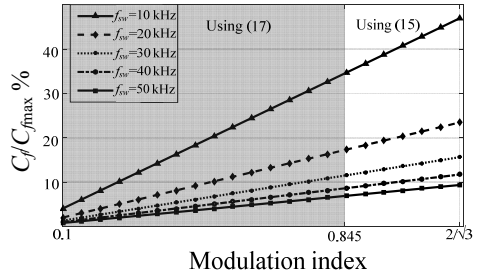

Fig. 6. Variation of the normalized filter capacitance with frequency and modulation index.

ΔQ. Therefore, the peak to peak voltage ripple (ΔV_{ripple}) can be written as follows.

At zero crossing, the filter capacitor voltage ripple is:

$$\Delta V_{ripple} = \frac{\Delta Q_{\text{zero current}}}{C_f} = \frac{1}{C_f}\frac{1}{2}\frac{\Delta i_{peak}}{2}\left(2T_2\right), \quad \left(T_2 = m_a\sqrt{3}/\left(8f_{sw}\right)\right) \tag{14}$$

If instead of Δi_{peak}, (5) is replaced in (14) then the voltage ripple is achieved as follows:

$$\Delta V_{ripple} = m_a^{\,2}\frac{V_{dc}}{64L_c f_{sw}^{\,2}C_f} \tag{15}$$

Similarly, for the peak current the voltage ripple is approximately defined as follows:

$$\Delta V_{ripple} = \frac{\Delta Q_{\text{peak current}}}{C_f} \approx \frac{1}{C_f}\frac{1}{2}\frac{\Delta i_{peak}}{2}\left(T_1 + T_2\right) \tag{16}$$

where $(T_1+T_2) = (1+m_a)/(4f_{sw})$. In (16), if Δi_{peak} is replaced by (6), then the voltage ripple is achieved as follows:

$$\Delta V_{ripple} \approx \left(1 - m_a/2\right)\left(1 + m_a\right)\frac{V_m}{32L_c f_{sw}^{\,2}C_f} \tag{17}$$

Therefore, depending on the modulation and the maximum allowed voltage ripple, the minimum required filter capacitance can be determined.

Normally, current ripple is considered k_1% (between 10-30% of nominal current) and voltage ripple is considered lower than k_2% (normally 5% of the nominal ac voltage). Replacing these values in (14) and (16), and normalizing them with respect to $C_{f,\max}$, then the normalized minimum filter capacitance is expressed as:

$$\frac{C_f}{C_{f,\max}} = \frac{10k_1}{k_2}\omega_g T \tag{18}$$

where T is the charging interval in one switching cycle (i.e. $2T_2$ for zero crossing and (T_1+T_2) for peak current according to (b)). Fig. 6 shows the variation of the minimum normalized filter capacitance. In this illustrative figure, for $m_a \le 0.845$, normalized C_f is calculated according to the analysis of the peak current and for $0.845 < m_a \le 1.15$, (18) is calculated based on the analysis of the zero crossing.

C. Damping resistor

From Fig. 1(b), the admittance from the converter side point of view is obtained as follows:

$$Y_{eq} = \frac{i(s)}{v_{an}(s)} = \Big/\left(\left(Z_{L_g} + Z_{L_f}\right)\Big\|Z_{C_f}\right) + Z_{L_c} \tag{19}$$

The admittance for a simple damping resistor R_d in series with the filter capacitor C_f is:

$$Y_{eq} = \frac{C_f\left(L_f + L_g\right)s^2 + R_d C_f s + 1}{C_f L_c\left(L_f + L_g\right)s^3 + R_d C_f L_T s^2 + L_T s} \tag{20}$$

where L_T is the total inductance (L_c+L_f+L_g). The higher limit of the damping resistance can be found by calculating the breakaway point of the root-locus as follows [see Fig. 7(c)]:

$$R_{d,\max} = \frac{2}{C_f}\sqrt{L_c\left(L_g + L_f\right)C_f/L_T} = \frac{2}{C_f\omega_n} \tag{21}$$

And the lower limit is found when $\xi = \sqrt{2}/2$ as follows:

$$R_{d,\min} = \sqrt{2L_c\left(L_g + L_f\right)/L_T C_f} \tag{22}$$

To reduce the power loss in the damping branch, filter capacitor C_f will be put in parallel with R_dC_d as shown in Fig. 7(b). From the root-locus analysis of this case [see in Fig. 7(d)], increasing the filter capacitance needs more damping resistance (higher loss). Increasing the damping capacitance (C_d) leads to have more stable system with lower damping

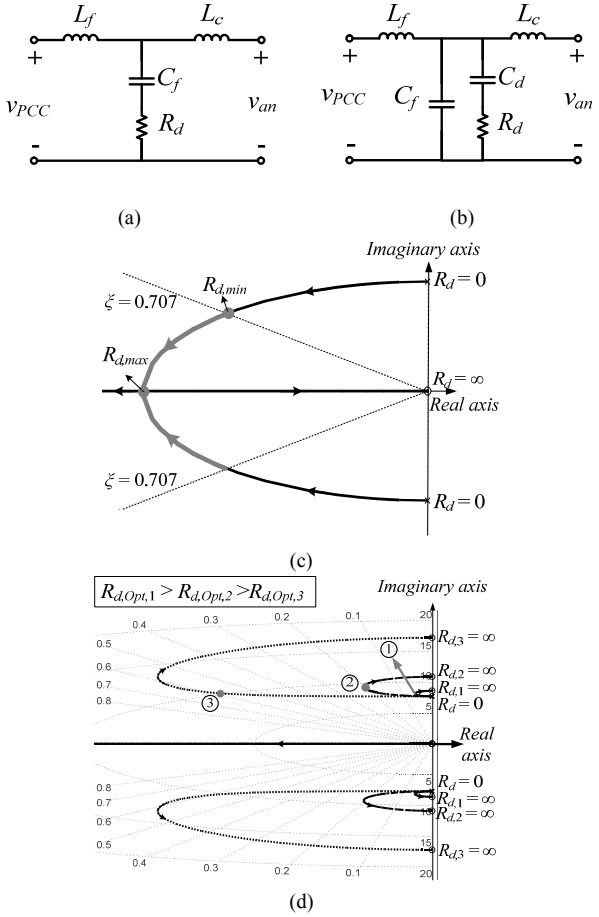

Fig. 7. (a) *LCL* filter with resistive damping, (b) *LCL* filter with RC damping, the corresponding root-locus for (c) finding an optimum damping resistor, (d) three different scenarios where 1) $C_f = 4C_d$, 2) $C_f = C_d$, 3) $C_f = 1/4C_d$ (in all scenarios C_f+C_d is kept constant).

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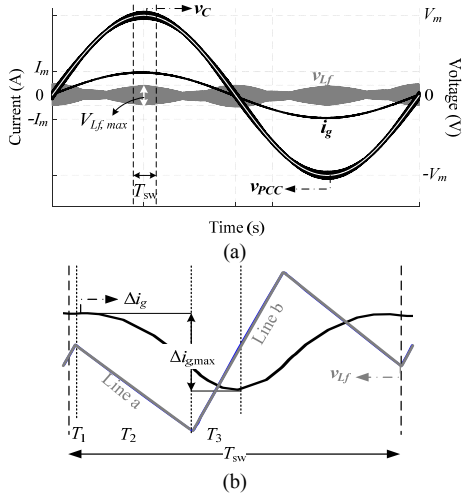

Fig. 8. The grid-side inductor (a) current and voltage and (b) magnified maximum inductance voltage and current in one switching cycle.

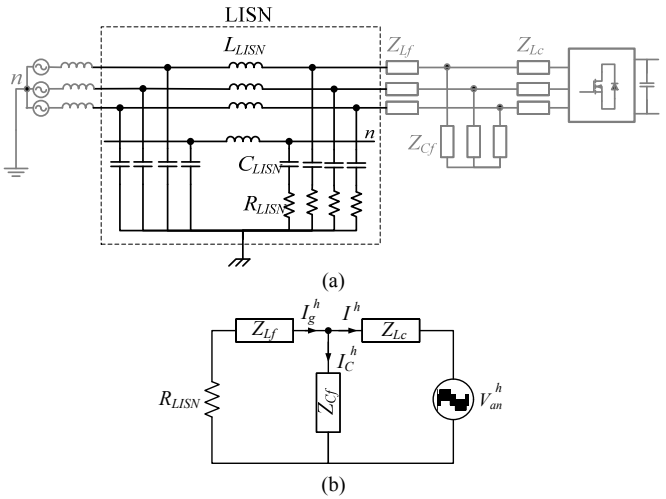

Fig. 9. (a) three-phase PFC with LISN equivalent circuit, and (b) single phase equivalent circuit of the filter at h^{th} harmonic with LISN ($h \geq 180$).

resistance, but attenuation after the resonance frequency reduces. As it is concluded in literature review [13]-[11], the best configuration is to keep both filter and damping capacitors identical.

D. Grid-side filter inductor

1) Method 1

The first method is using the filter configuration shown in Fig. 7(a). The capacitor ideally draws the high frequency current harmonics. If the damping resistor is correctly chosen, the impedance of the damping branch is still smaller than the impedance of the grid-side filter inductance at switching side-band frequency. By adding the damping resistor, the grid-side filter inductor voltage is influenced by the current ripple flowing through the filter capacitor.

Fig. 8(a) shows the common coupling, the damping branch, and the grid-side filter inductor voltages along with the grid current. The grid-side filter inductor voltage is proportional to the converter-side inductor current ripple by comparison of Fig. 8(b) and Fig. 4(b), hence it can be written as follows:

$$v_{L_f} \propto R_d \Delta i \tag{23}$$

Equation (23) implies that the voltage across the grid-side filter inductance is a function of the damping resistance and the converter current ripple. To express (23) more accurately, the corresponding voltage line equation for line "*a*" and "*b*" in Fig. 8(b) is found as follows:

$$v_{line(a)}(t) = \frac{R_d}{L_c}\left(\left(m_a V_m - 2V_{dc}/3\right)\left(t - T_1\right) + m_a V_m T_1\right) \tag{24}$$

$$v_{line(b)}(t) = \frac{R_d}{L_c}\left(m_a V_m\left(t - T_2 - T_1\right) + \left(m_a V_m - 2V_{dc}/3\right)T_2 + m_a V_m T_1\right) \tag{25}$$

Therefore, the grid-side filter inductance value using the basic equation of the inductor voltage (e.g. (2)) is achieved as (26).

$$L_{f,\min} \approx R_d \frac{\Delta i_{peak}}{18 f_{sw} \Delta i_g^*}\left(1 + m_a\right) \tag{26}$$

where Δi_g^* is the maximum allowable current ripple at the grid side with respect to the grid standards. Using (22) and (26), the values for R_d and L_f can be calculated. The minimum grid filter inductance has only been derived for the peak current. The method can be extended for the zero-crossing. However, the achieved results in both cases are close. Therefore, (26) is reasonably adequate for finding the grid filter inductance.

2) Method 2

The attenuation of the configuration shown in Fig. 7(b) is higher than the previous configuration and the high frequency grid current ripple is almost negligible.

Designing this filter parameter often ends up with oversizing of grid-side filter inductor. Providing well-defined grid impedance which is defined by the standards can be beneficial for having an optimum filter and repeatable measurements. By introducing the WBG switches, the switching frequency of converters are increased which means the major converter current harmonics drops at high frequency where LISN can provide well-defined impedance. The three-phase PFC using LISN equivalent circuit is shown in Fig. 9 with the single-phase equivalent circuit of filter for high frequency current ripple ($h \geq 180$). In fact, LISN provides the only valuable impedance which is defined by the standards. Therefore, finding the grid-side filter inductance is only achievable by LISN. By analyzing the equivalent circuit, the grid-side filter inductance is achieved.

In (27), all the parameters are known such as filter capacitance, converter-side inductance, and the LISN resistance. The converter harmonic voltage is also known by FFT of v_{an} at switching side-band frequency.

$$L_f = \left(\sqrt{\left|\frac{V_{an,h}}{I_{g,h}^*}\right|^2 - \left(R_{LISN}\alpha\right)^2}\right| - L_c\omega_h\Bigg) \Big/ \alpha\omega_h \tag{27}$$

$$\alpha = C_f L_c \omega_h^2 - 1$$

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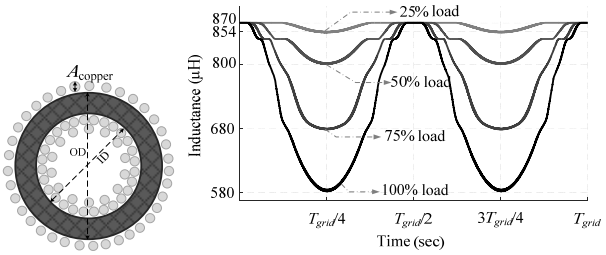

Core: MPP C055439A2
Number of turns: 82, Number of layers: 1.5
A_{copper}: 1.42 mm, OD: 46.7 mm, ID: 24.1 mm
DC copper resistance: 74 mΩ

Fig. 10. Schematic of the toroidal core, and the inductance change through fundamental frequency of main current for different loads

IV. Results and Discussion

To verify the proposed filter design methods, two *LCL* filters are designed for a 5 kW SiC based three-phase PFC. The converter is connected to a grid simulator (A 5.5 kVA grid simulator- California instrument CSW5550) to observe the performance of the converter under different conditions. The current control is designed by the proportional- resonant (PR) controller in the $\alpha\beta$ stationary reference frame and implemented in dSPACE system. Two case studies have been taken 1) the filter configuration I [shown in Fig. 7(a)] and 2) the filter configuration II [shown in Fig. 7(b)]. All the measurements are done using LISN to make sure the measurements are repeatable.

According to the specification of the converter, by considering 30% current ripple as the limit for the converter-side inductance and using (5), the inductor L_c becomes 580μH for 700 V dc link voltage (the highest dc link voltage determines the largest required inductor). MPP toroidal core has been utilized for this inductor. A great attention has been dedicated to the saturation flux density, the size and the number of winding. The specifications of the inductor are shown in Fig. 10. Since, MPP features a soft saturation behavior like the other powder cores family, the inductance value changes by changing the main current through the fundamental frequency of the grid. Fig. 10 shows the change in the inductance value for different load conditions.

For no-load or grid current lower than 2 A, the inductance value is 870 μH. As soon as the instantaneous current increases (more than 2 A), the inductance value starts to decrease. The full load inductance is about 580 μH. This variable inductance value causes a change in the profile of the current ripple.

The minimum filter capacitance having 5% of nominal ac voltage as voltage ripple is 0.45 μF (using (14) since $m_a >$ 0.845). The maximum filter capacitance using (13) is 5 μF. To reduce the grid-side filter inductance size the maximum filter capacitance is chosen. TABLE III lists the filter parameters for two configurations.

The converter-side inductance and the filter capacitance are identical for both of the configurations. The point of difference drops on the grid-side filter inductances and damping resistors which are calculated differently. Configuration I leads to 3 times larger inductance and consequently more number of turn, larger core and copper

TABLE III
THE FILTER PARAMETERS FOR CONFIGURATION I AND II

Parameters	Configuration I	Configuration II
Δi (A)	$30\%\times\sqrt{2}\times I_{nom} = 3$	
L_c (μH)	580 (Eq. (5))	
Δi_g (A)	0.2	—*
L_f (μH)	330 (Eq.(26))	100 (Eq.(27))
R_d (Ω)	10 (Eq.(22))	8
ΔV_{ripple} (V)	$5\%\times230\sqrt{2}$	
C_f (μF)	5 (Eq. (13)&(14))	2.5
C_d (μF)	0	2.5
$P_{loss,damping}$ (W)**	4	0.85

*Instead of current ripple, the current harmonic by the standard is used.
**Full load power loss.

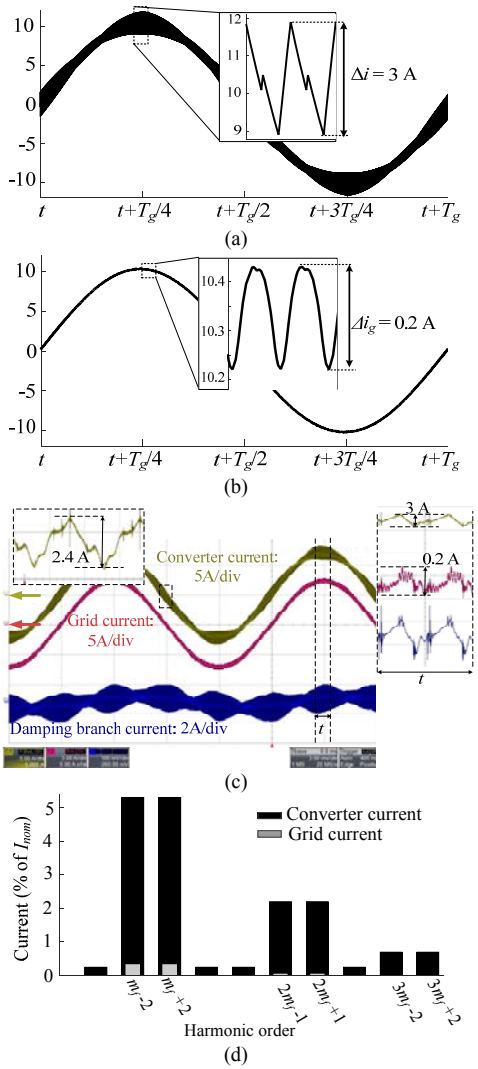

Fig. 11. Configuration I (a) and (b) simulated converter and grid current, (c) measured converter, grid, and damping branch current (d) measured harmonic comparison after and before filter.

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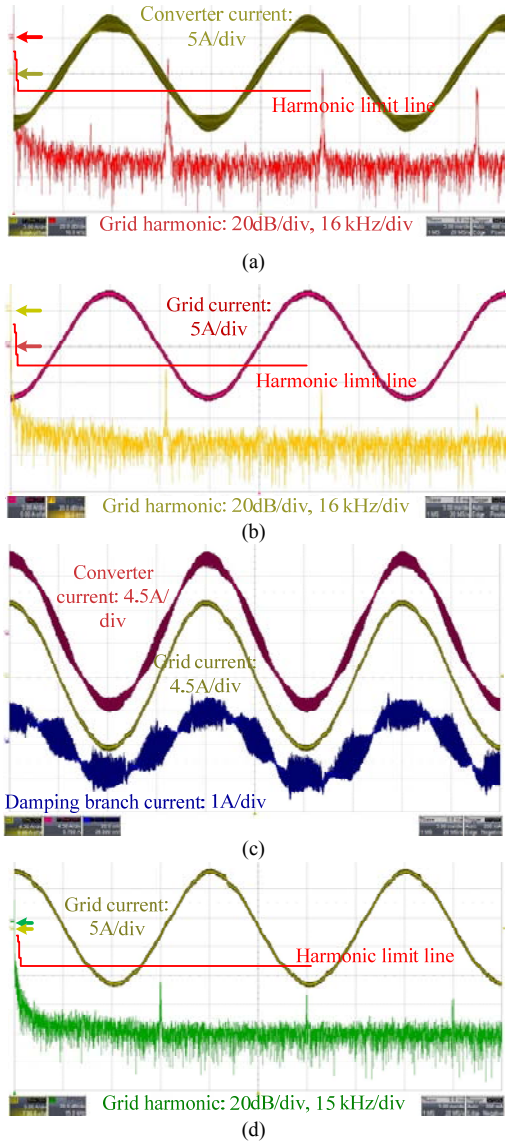

Fig. 12. Configuration I: the harmonic performance of the (a) converter current (b) grid current. Configuration II: (c) the current behavior of the filter capacitor, converter side inductor, and damping branch (d) grid current and its harmonic.

losses (note: both inductors of configurations are winded on the similar core). The flowing harmonic currents through the filter shunt branch are larger in configuration I and that leads to larger damping loss. Therefore, as known the power loss of configuration I is higher than II (as seen in TABLE III).

The simulation and experimental results for the first configuration are shown in Fig. 11 for 700 V dc link voltage. Fig. 11(a)&(b) demonstrates the simulated converter and the grid currents, respectively. Fig. 11(c) shows the measured converter, the grid and the damping branch currents. The converter and grid current ripple at peak confirm the analysis for linear modulation. According to the dc link voltage level, it is expected to see the maximum current ripple at zero-crossing. However due to the dc magnetization of the core material, the inductance value at zero crossing is about 870 µH while in the peak is equal to 580µH. Therefore, the current ripple at zero crossing is reduced accordingly while at peak it is increased.

Harmonic analysis of the current before and after the filter demonstrates sufficient attenuation at especially switching side-band harmonics [see Fig. 11(d)]. The harmonic performance of the converter and the grid current are also shown in Fig. 12(a)&(b). For configuration II, the same experiments are done and the results are shown in Fig. 12(c) & (d). There is a substantial different between two configurations with respect to the current flowing through the damping resistor as it can be seen in Fig. 11(c) and Fig. 12(c). Moreover, by comparison of the FFT of the grid current in both configurations, it is clear that the current is attenuated more in the second configurations. Although, the grid-side filter inductance is smaller in the configuration II, the grid current harmonics are also smaller at side-band switching frequency due to the essential difference on the shunt branch of two configurations.

V. Conclusion

This paper has presented a comprehensive analytical method for designing *LCL* filter of a three-phase power factor correction rectifier (PFC). The method is explained by the converter current and the voltage behavior. The converter current ripple determines all the filter parameters and defines a suitable margin for them. A general equation is derived for the maximum converter current ripple which is applicable for sinusoidal PWM and third-harmonic injection PWM. The analysis is performed for unity power factor. It is proved that for modulation index higher than 0.845 the maximum current ripple occurs at zero crossing otherwise it appears at peak current. Consequently, the maximum charge of the filter capacitor is analytically obtained. Unlike the normal method on the literature in which the maximum filter capacitance is defined by absorbed reactive power. In this paper, the minimum filter capacitance is chosen according to the converter current analysis. Two methods are proposed for deriving the grid-side filter inductance. The first method uses the properties of the damping method and derives the required grid-side inductance as a function of the damping resistor and the converter current ripple. The second method focuses on reducing the power loss in the filter and optimizing it by employing line impedance stabilization network (LISN). Since in this paper, silicon-carbide switches (SiC) are used for designing the converter, consequently the switching frequency is in the order of couple of 10 kHz. Therefore, LISN can actively provide well-define impedance for switching side-band harmonics. Using LISN easily gives the grid-side filter inductance independent from the grid impedance. Two *LCL* filters for the 5 kW three-phase SiC based PFC have been designed and tested for different scenarios. The experimental results are match with the analysis.

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