Dummy Gate-Assisted n-MOSFET Layout for a Radiation-Tolerant Integrated Circuit

Min Su Lee and Hee Chul Lee

***Abstract*—A dummy gate-assisted n-type metal oxide semiconductor field effect transistor (DGA n-MOSFET) layout was evaluated to demonstrate its effectiveness at mitigating radiation-induced leakage currents in a conventional n-MOSFET. In the proposed DGA n-MOSFET layout, radiation-induced leakage currents are settled by isolating both the source and drain from the sidewall oxides using a p+ layer and dummy gates. Moreover, the dummy gates and dummy Metal-1 layers are expected to suppress the charge trapping in the sidewall oxides. The inherent structure of the DGA n-MOSFET supplements the drawbacks of the enclosed layout transistor, which is also proposed in order to improve radiation tolerance characteristics. The $V_g - I_d$ simulation results of the DGA n-MOSFET layout demonstrated the effectiveness of eliminating such radiation-induced leakage current paths. Furthermore, the radiation exposure experimental results obtained with the fabricated DGA n-MOSFET layout also exhibited good performance with regard to the total ionizing dose tolerance.**

***Index Terms*—Dummy gate-assisted n-MOSFET layout, layout modification, radiation hardening, radiation-induced leakage current, total ionizing dose.**

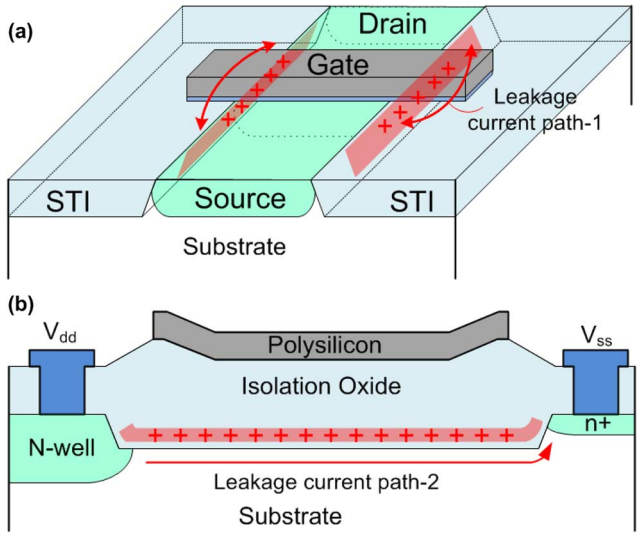

Fig. 1. Possible radiation-induced leakage current paths (a) through the source-to-drain area along the sidewall oxide and (b) between two components under the isolation oxide.

I. Introduction

SPACE applications such as space shuttles and satellites require radiation-tolerant application-specific integrated circuits. Outer space contains numerous radiation sources, including the Van Allen belt, solar flares, and cosmic rays [1]. When complementary metal oxide semiconductor (CMOS) integrated circuits are operated in a high radiation environment such as outer space, they are subjected to numerous types of anomalies [2], [3]. In severe cases, these radiation-induced anomalies can cause a system to lose all functionality [4], [5].

Among these radiation-induced anomalies, the total ionizing dose effect, which corresponds to long-term accumulated radiation damage, generally worsens the performance of CMOS integrated circuits by altering the characteristics of the n-type metal oxide semiconductor field effect transistors (n-MOSFETs) contained in the circuits [6]. Therefore, CMOS integrated circuits used in space for long-term missions should have radiation-tolerant n-MOSFETs in order to mitigate or eliminate the total ionizing dose effects.

In n-MOSFETs, the total ionizing dose effects result from the trapping of the radiation-induced holes at the silicon-silicon dioxide interface [6]. Furthermore, according to recent reports [7], [8], for n-MOSFETs fabricated using a deep sub-micron process with a gate oxide that has a thickness of less than 10 nm, two types of leakage current paths may occur by radiation-induced trapped charges. The problems tend to disappear underneath the gate oxide, because radiation-induced holes are not trapped in oxides with thickness of less than 10 nm; they are only trapped in thick oxides such as sidewall oxides and isolation field oxides. As a result, radiation-induced leakage current paths are formed along the sidewall oxides and under the isolation field oxides, causing greater system noise and power consumption [9]. Fig. 1 presents these two possible radiation-induced leakage current paths in CMOS integrated circuits fabricated via the commercial deep sub-micron process [10].

Several transistor layouts have been reported and evaluated for the purpose of eliminating these radiation-induced leakage current paths. Among these layouts, the enclosed layout transistor (ELT), which has been widely investigated due to its high radiation-tolerant characteristics, performs well even with a very high total dose of radiation up to 30 Mrad (SiO_2)

Manuscript received December 04, 2012; revised March 08, 2013 and May 02, 2013; accepted June 05, 2013. Date of publication July 09, 2013; date of current version August 14, 2013. This work was supported by a project of the Ministry of Education, Science and Technology (development of radiation hardening design technology of MOSFET, ADC and SRAM for satellites) and the IC Design Education Center in Korea Advanced Institute of Science and Technology.

The authors are with the Division of Electrical Engineering, School of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: goodaaaa@kaist.ac.kr; hclee@kaist.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNS.2013.2268390

[11]–[13]. However, the use of the ELT requires trade-offs. The ELT has limitations with regard to its width over length (W/L) ratio, complex W/L ratio modeling, asymmetrical geometry, and large gate capacitance [13], [14]. The limitation with regard to the W/L ratio, which is that it is not possible to have a W/L ratio smaller than 2.26 [13], is a significant concern in analog circuit designs [14] such as image sensor readout integrated circuits, which often use a small W/L ratio. In addition, the larger gate capacitance is also a significant concern for digital circuits because it increases the timing delay and thus reduces the upper limit of the clock frequency. Therefore, very high-speed digital systems thus far remain unrealized for radiation-tolerant circuits using the ELT [13], [14].

In order to overcome these drawbacks in the ELT, the new dummy gate-assisted (DGA) n-MOSFET layout was proposed [15]. This study evaluates the radiation-tolerant effectiveness of the new DGA n-MOSFET layout through a device simulation and radiation exposure experiment. Furthermore, the manner in which the DGA n-MOSFET layout supplements the drawbacks in the ELT is discussed.

II. Proposed DGA n-MOSFET Structure

A. Layout Description

Fig. 2(a) and 2(b) show a conventional n-MOSFET layout and the proposed DGA n-MOSFET layout, respectively. The conventional n-MOSFET layout consists of an N-active layer, a gate-poly layer, and an $\mathrm{n+}$ implant layer. Compared with the conventional n-MOSFET layout, the proposed DGA n-MOSFET layout has two additional side dummy-gate layers, dummy Metal-1 layers, P-active layers, and $\mathrm{p+}$ layers. The source and drain of the proposed n-MOSFET layout are isolated from the sidewall oxides using these additional layers to block any possible radiation-induced leakage current. Moreover, when isolating the source and drain from the sidewall oxides, the dummy gate is adopted as a priority because the dummy gate occupies a smaller area compared with that of the P-active layer involving the $\mathrm{p+}$ layer.

The primary role of both sides of the dummy gate is separating the source and drain from the sidewall oxides. The radiation-induced holes are not trapped under the dummy gates. This is because if the gate oxide thickness is less than 10 nm, the holes are not trapped at the silicon-silicon dioxide interface [7], [8]. Therefore, the dummy gates can block the possible pathways of the radiation-induced leakage current.

Another minor additional positive effect from both sides of the dummy gate can be achieved by applying a flat band voltage $(\mathrm{V_a})$ to the dummy gates. If a zero electric field is applied to oxides, the hole trapping is minimized [16], [17]. The minimum hole trapping under the sidewall oxides leads to the prevention of radiation-induced leakage currents. However, this effect is not absolutely necessary because even though the radiation-induced holes are trapped in the sidewall oxides, the dummy gates still block the radiation-induced leakage current. Furthermore, in most cases, the voltage $(\mathrm{V_a})$ is recommended to be zero even when the flat band voltage is not zero. This is because only when the voltage of $\mathrm{V_a}$ is zero, it ensures no additional net gate-to-substrate leakage currents and no electrical anomalies affecting operation of the transistor.

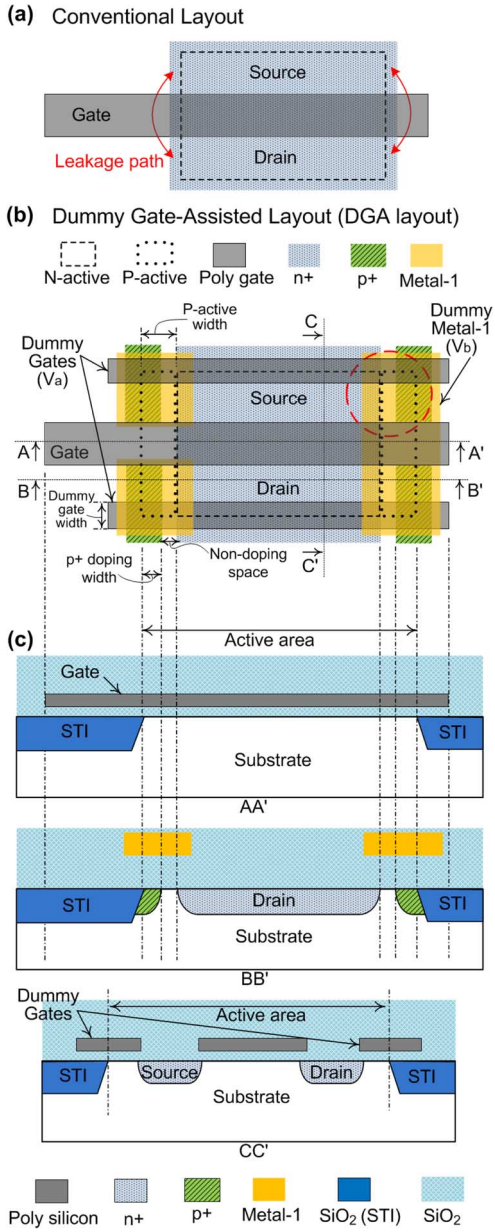

Fig. 2. (a) Conventional n-MOSFET layout, (b) proposed DGA n-MOSFET layout, and (c) cross-sections of the DGA n-MOSFET layout.

The sides of the source and drain, which the dummy gates do not surround, are covered with $\mathrm{p+}$ layers and dummy Metal-1 layers. The radiation-induced trapped charges can be formed under the passivation oxide between the dummy Metal-1 layer and the substrate. Furthermore, this will cause the leakage current between the source and drain to pass through a possible inverted channel. Therefore, $\mathrm{p+}$ layers are adopted in this region in order to prevent these possible leakage current paths. It is known that a high $\mathrm{p+}$ doping layer can prevent the channel inversion induced by the positive trapped charges [18].

The dummy Metal-1 layer, which is connected to $\mathrm{V_b}$, is used to mitigate the generation of radiation-induced trapped charges in the passivation oxide between the dummy Metal-1 layer and

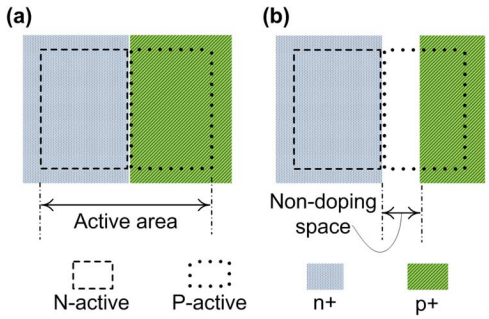

Fig. 3. Detailed view of the red-circled region in Fig. 2(b): (a) butted contact between the N-active layer and P-active layer, which was allowed according to the design rule for when both sides have the same potential. (b) Modified butted layout for the difference potential, where the n+ side could be applied to the VDD or a certain voltage when the p+ side was connected to the GND.

the substrate. V_b is a specified flat band voltage that creates a zero electric field in the passivation oxide. Therefore, radiation-induced trapped charge generation under the dummy Metal-1 layer can be suppressed. Consequently, with the p+ doping layer, the possible radiation-induced leakage current is expected to be effectively suppressed under the dummy Metal-1 layer. It should be noted that the effects on the p+ layer and dummy Metal-1 layer are discussed separately in a later paper.

Fig. 2(c) presents the cross-sections of the proposed DGA n-MOSFET layout. From Fig. 2(c), it can be seen that the proposed DGA n-MOSFET layout does not have contacts between the source or drain, and the sidewall oxides. As a result, the source and drain are fully isolated from all radiation-induced trapped charges; thus, it is expected that all possible leakage current paths will be eliminated.

B. Consideration of Layout Drawing

In the DGA n-MOSFET layout, the dummy gate poly layers could be located inside the active area by extending the active layers in the CC' direction, for a case in which an active layer beyond a poly layer is not permitted in a given fabrication process. Additionally, this modification will not affect the radiation tolerance characteristics of the proposed layout because the dummy gate still blocks the radiation-induced leakage current path.

Fig. 3 presents a detailed view of the region circled in red in Fig. 2(b). In this research, along with the design rules provided by MagnaChip & Hynix, the butted layout shown in Fig. 3(a) was allowed when both the N-active and P-active components had the same potential. The butted contact shorts the path between the n+ region and p+ region due to band-to-band tunneling. However, in the proposed layout, the N-active region serves as the source or drain, which could be applied to a certain voltage between VDD and GND. In order to address this problem, a non-doping space between the n+ layer and p+ layer was formed by reducing the p+ layer, while the P-active layer has no change. This modification also prevents the formation of shallow trench isolation (STI) field oxides at the non-doping space between the p+ layer and n+ layer, because the P-active layer remains in the space. This is important because if an STI field oxide forms at the non-doping space, it will cause radiation-induced leakage currents along the STI sidewall oxides.

TABLE I
INCREASING RATIOS OF GATE CAPACITANCES AND AREAS OF THE DGA N-MOSFETS COMPARED WITH CONVENTIONAL N-MOSFETS

Width	Length	Increasing ratio of gate capacitance	Increasing ratio of area
1 μm	0.44 μm	120 %	142 %
2 μm	0.44 μm	60 %	97%
3 μm	0.44 μm	40 %	78%
1 μm	1 μm	120 %	128%
2 μm	1 μm	60 %	85%
3 μm	1 μm	40 %	67%
1 μm	2 μm	120 %	114%
2 μm	2 μm	60 %	74%
3 μm	2 μm	40 %	58%
1 μm	3 μm	120 %	107%
2 μm	3 μm	60 %	69%
3 μm	3 μm	40 %	52%

The p+ layer should not extend above the transistor gate. If it does, a p-n junction can be formed on the transistor gate. Furthermore, the p-n junction will result in the DGA n-MOSFET being turned off slowly, because the state of the p-n junction is reverse bias when the gate voltage changes from high to low. Therefore, in order to prevent this effect, the p+ layer should not be extended above the transistor gate.

The size of each additional layer depends on the process design rules. Nevertheless, it is recommended to make the size of each additional layer greater than the minimums suggested in the design guidelines, because each of the additional layers should also block radiation-induced leakage currents.

C. Structural Characteristics

The inherent geometric characteristics of the proposed n-MOSFET layout will ensure a symmetric geometry and smaller gate capacitance than the ELT, while also ensuring that limitations are not imposed on the W/L ratio. Compared with a conventional n-MOSFET, the increase of the gate capacitance in the proposed layout depends on the additional P-active layer width or allowed minimum P-active layer width. Along with the design guidelines used in this study, a comparison of the gate capacitances between the conventional n-MOSFET and proposed DGA n-MOSFET is presented in Table I. For the DGA n-MOSFET, the side dummy gate width, P-active width, and p+ doping width were 0.4 μm, 0.6 μm, and 0.3 μm, respectively. The gate capacitance of the DGA n-MOSFET was significantly smaller relative to that of the ELT, especially when the W/L ratio was minimized.

In addition, the source and drain of the DGA n-MOSFET were fully isolated from any radiation-induced trapped charges. Thus, additional p+ guard ring isolation is not required to prevent leakage current paths between the transistor cells. This indicates that the proposed layout occupies a smaller area than layouts that require p+ guard ring isolation. This smaller footprint is another benefit of the proposed DGA n-MOSFET layout.

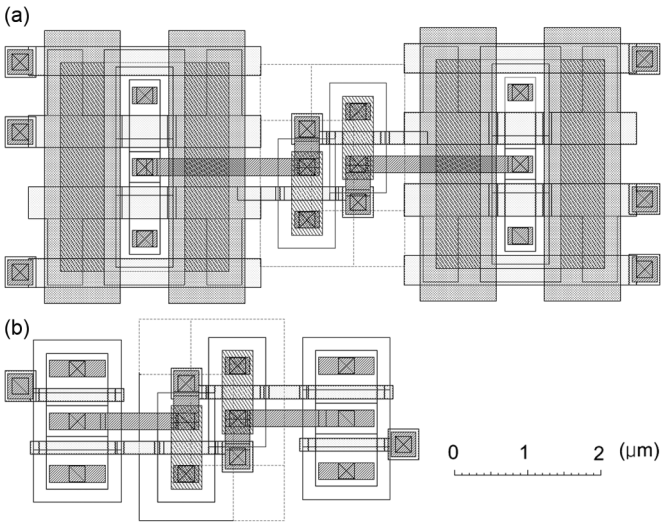

Fig. 4. Comparison between areas of the SRAM layouts with (a) the DGA n-MOSFET and with (b) a conventional n-MOSFET using MagnaChip & Hynix 0.18 μm process technology.

Along with the design guidelines used in this study, a comparison of the total areas occupied by the conventional n-MOSFET and by the DGA n-MOSFET without an additional p+ guard ring structure is also shown in Table I. The area occupied by the DGA n-MOSFET is much smaller relative to the ELT, especially when the W/L ratio is minimized.

D. Layout Compatibility

In regard to scaling, it is expected that the DGA n-MOSFET can be fabricated using advanced fabrication processes. Compared with a conventional n-MOSFET, the DGA n-MOSFET requires three additional masks: the P-active layer, p+ layer, and Metal-1 layer. However, these additional masks are already used in the fabrication of p-MOSFETs. As a result, if the n-MOSFET and p-MOSFET fabrication processes are combined, the DGA n-MOSFET can be realized without extra masks and without consideration of the minimum feature sizes for a given fabrication process.

Generally, digital circuits use transistors with a minimum gate length. The minimum gate length of the DGA n-MOSFET is limited by the minimum distance between the p+ layers. Moreover, the minimum distance between the p+ layers is generally larger than the minimum feature size provided by a given fabrication process. Therefore, the DGA n-MOSFET design can result in slower operating speeds in radiation-hardened digital circuits.

When a very large scale integration (VLSI) circuit design incorporates the DGA n-MOSFET, the foremost disadvantage is the area occupied, even though the DGA n-MOSFET occupies less area than an ELT layout. For example, when an SRAM unit cell is designed using the DGA n-MOSFET layout, the occupied area increases by approximately 116% compared with a SRAM unit cell layout with a conventional n-MOSFET. A comparison between the areas of the SRAM layouts with the DGA n-MOSFET and with the conventional n-MOSFET is shown in Fig. 4. Furthermore, a precise effective W/L ratio model for the DGA n-MOSFET should be developed in order to enhance circuit accuracy. It is expected that if the effective W/L ratio model for the DGA n-MOSFET is developed, the VLSI circuit can be designed in a conventional manner.

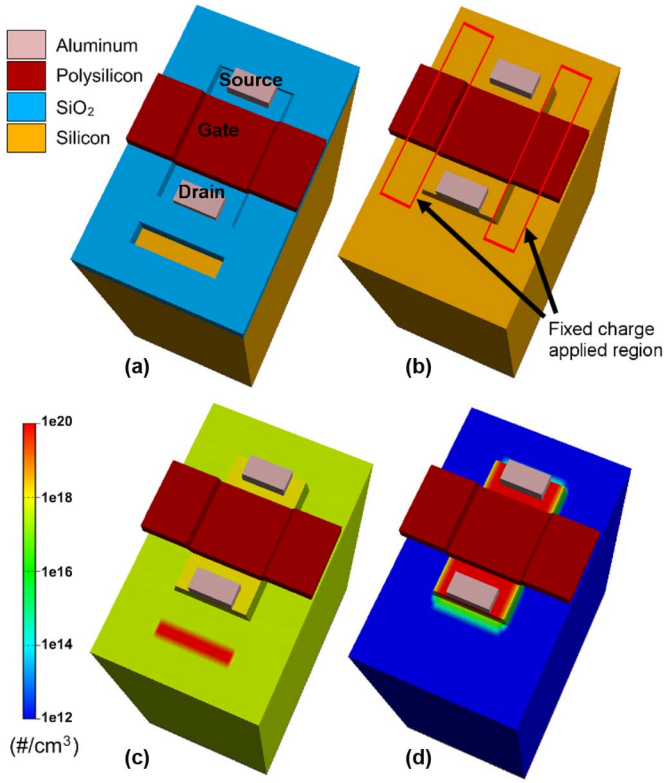

Fig. 5. The conventional n-MOSFET structure designed using the SILVACO ATLAS simulation tool. (a) Overall shape of the structure. (b) Fixed charge applied region. (c) p-doping concentration profile. (d) n-doping concentration profile with transparent configuration of the oxide in a log scale.

III. Simulation Results

A. Conventional n-MOSFET Structure

The conventional n-MOSFET structure shown in Fig. 5 was designed to be compatible with the commercial 0.18 μm process technology using the SILVACO ATLAS simulation tool. The W/L ratio, gate oxide thickness, and body thickness were 1 μm/1 μm, 4 nm, and 6 μm, respectively. Fig. 5(c) and 5(d), in which the oxide volume was configured to be transparent for convenient evaluation of the doping concentration, present the p-doping concentration and n-doping concentration profiles, respectively, in the silicon substrate in a log scale. The channel region was doped higher than the substrate body in order to adjust the threshold voltage and to reduce the off-current.

When the total ionizing dose effect was simulated in the designed structures, the fixed charge density was adjusted on the sidewall oxide. When a CMOS device is exposed to radiation, hole trapping results in fixed charges and interface states in the thick oxides. According to a report on the radiation-induced fixed charge density and interface state density in MOS capacitors [19], the radiation-induced flat band voltage is dominantly shifted by the fixed charges. The effect of the interface states is minor. Therefore, in this simulation, the interface states were

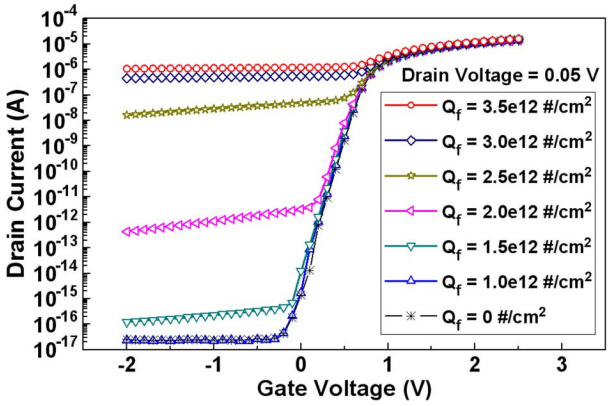

Fig. 6. Simulation results of the $\mathrm{V_g} - \mathrm{I_d}$ curve of a conventional n-MOSFET with changes in the fixed charge density on the sidewall oxide between the source and drain. The simulation was performed with a drain-to-source voltage of 0.05 V; the W/L ratio of the n-MOSFET was 1 μm/1 μm.

neglected and only the fixed charge density was modified to reflect the total ionizing dose effect.

Fig. 6 presents the simulation results of the $\mathrm{V_g} - \mathrm{I_d}$ curve of the conventional n-MOSFET with changes in the fixed charge density on the sidewall oxides between the source and drain. The sidewall oxide interface region, in which the fixed charge density was changed, is indicated using red boxes in Fig. 5(b). The gate bias was swept from -2 V to 2.5 V in order to evaluate the fixed charge-induced leakage current and the on current change. Fig. 6 demonstrates that the leakage current increased as expected with the increases of the fixed charge density on the sidewall oxides. It was also noted that the on current increased slightly as the fixed charge density on the sidewall oxides increased.

B. Proposed DGA n-MOSFET Structure

Using the SILVACO ATLAS simulation tool, the proposed DGA n-MOSFET structure shown in Fig. 7 was designed to be compatible with the MagnaChip & Hynix 0.18 μm process technology. The side dummy gate width, P-active width, and p+ doping width were 0.4 μm, 0.6 μm, and 0.3 μm, respectively. Each size was determined in accordance with the given process design guidelines. Fig. 7(c) and 7(d), in which the oxide volume was configured to be transparent for convenient evaluation of the doping concentration, present the p-doping concentration and n-doping concentration profiles, respectively, in the silicon substrate in a log scale. The simulation adopted a relatively low-doped p+ layer for a doping concentration of 1e19 #/cm^3 as a blocking layer against the fixed charge-induced leakage current.

However, the SILVACO ATLAS simulation tool was not able to simulate the electric field dependency during radiation exposure. Therefore, the suppression of the hole trapping under the dummy gates and dummy Metal-1 layers was not considered in this simulation. Furthermore, the fixed charge density was increased to that expected in a conventional n-MOSFET situation in order to evaluate the worst-case scenario when the fixed charge density was saturated.

Fig. 8 presents the simulation results of the $\mathrm{V_g} - \mathrm{I_d}$ curve of the proposed DGA n-MOSFET with changes in the fixed charge density on the sidewall oxides between the source and drain. The sidewall oxide interface region, in which the fixed charge density was changed, is indicated using the red boxes in Fig. 7(b). Fig. 8 demonstrates that the leakage current was nearly unchanged, as expected, as the fixed charge density on the sidewall oxide increased. These simulation results imply that the proposed DGA n-MOSFET layout effectively eliminates the positive fixed charge-induced leakage current paths.

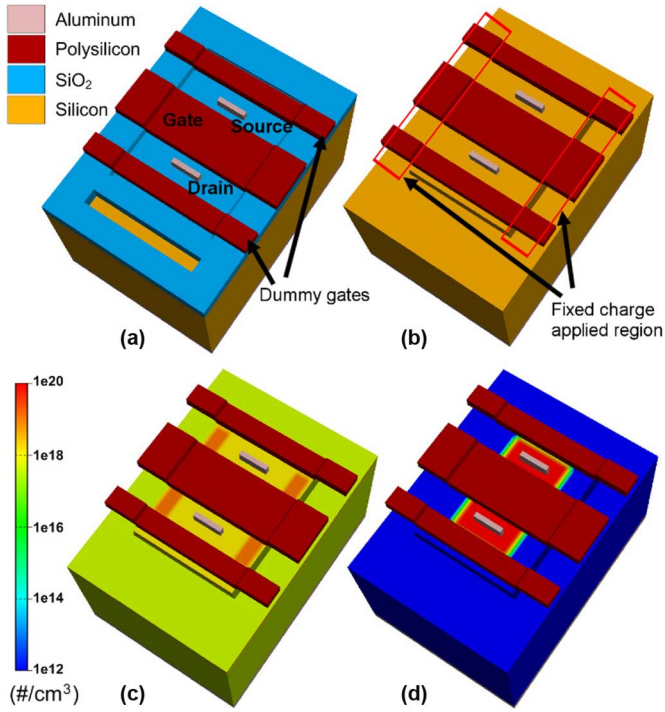

Fig. 7. The proposed DGA n-MOSFET structure designed using the SILVACO ATLAS simulation tool: (a) overall shape of the structure. (b) Fixed charge applied region, (c) p-doping concentration profile, and (d) n-doping concentration profile with transparent configuration of oxide in a log scale.

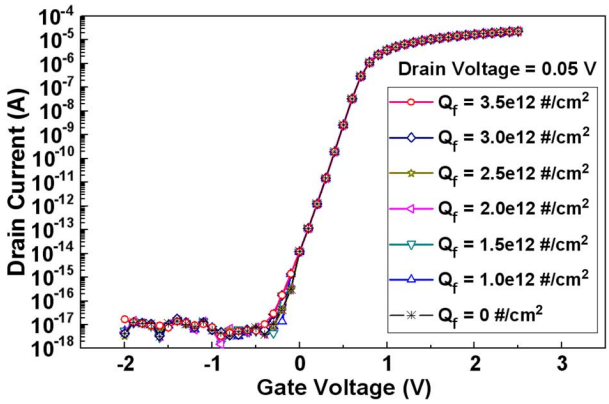

Fig. 8. Simulation results of the $\mathrm{V_g} - \mathrm{I_d}$ curve of the proposed DGA n-MOSFET with changes in the fixed charge density on the sidewall oxide between the source and drain. The simulation was performed with a drain-to-source voltage of 0.05 V; the W/L ratio of the n-MOSFETs was 1 μm/1μm.

IV. Experimental Results

A conventional n-MOSFET and the proposed DGA n-MOSFET layout were fabricated using MagnaChip & Hynix 0.18 μm technology with a gate oxide thickness of less

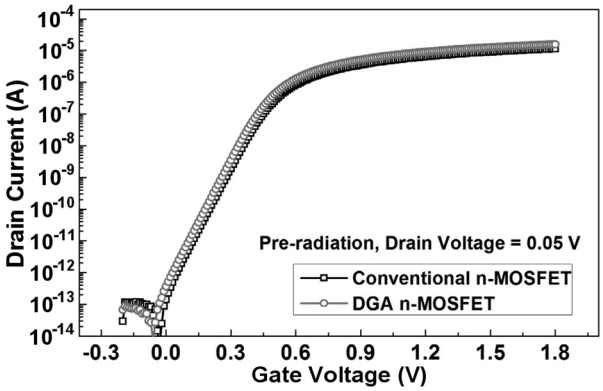

Fig. 9. Comparison of the $V_g - I_d$ characteristic between the conventional n-MOSFET and the proposed n-MOSFET prior to irradiation. The measurement was taken with a drain-to-source voltage of 0.05 V; the W/L ratio of the n-MOSFETs was 1.2 μm/1.2 μm.

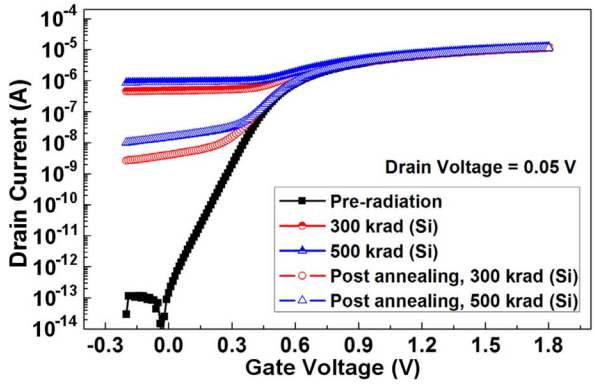

Fig. 10. Experimental results for the $V_g - I_d$ curve of the conventional n-MOSFET before and after irradiation for total doses of 300 krad (Si) and 500 krad (Si) given at the same dose rate of 100 krad/h. The measurement was taken with a drain-to-source voltage of 0.05 V; the W/L ratio of the n-MOSFETs was 1.2 μm/1.2 μm.

than 5 nm, an STI to isolate the active areas, and a Metal-1 layer of aluminum. It should be noted that the proposed DGA n-MOSFET layout violated the design guidelines from MagnaChip & Hynix. The design rule violation occurred near the p+ layer because this area was treated as a p-MOSFET. However, the area near the p+ layer does not operate as a p-MOSFET. MagnaChip & Hynix agreed with this explanation and approved the fabrication of the proposed DGA n-MOSFET layout.

The test chip had two types of W/L ratios (4 μm/1 μm and 1.2 μm/1.2 μm) for both the conventional n-MOSFET and the proposed DGA n-MOSFET. In order to evaluate the radiation-induced leakage current between the two different transistors, two devices were positioned with a distance of 3 μm between one p-n junction edge and the other p-n junction edge for both n-MOSFETs. Moreover, the Metal-1 layer, named as field Metal-1, was drawn between these two p-n junctions as overlapping each p-n junction. Finally, the fabricated test chips were packaged.

The measurement results shown are for the W/L ratio of 1.2 μm/1.2 μm only. The n-MOSFETs for both W/L ratios of 4 μm/1 μm and 1.2 μm/1.2 μm exhibited almost the same characteristics. Furthermore, all measured $V_g - I_d$ curves shown in Figs. 9 to 11 are from a single sample.

A comparison of the $V_g - I_d$ characteristics between the conventional n-MOSFET and the proposed DGA n-MOSFET is shown in Fig. 9. There was a slight difference at the threshold voltage of approximately 0.02 V. However, in the given fabrication process, the threshold voltage variation was about 0.07 V. Therefore, it can be understood that the differences in the electrical characteristics between the conventional n-MOSFET and the proposed DGA n-MOSFET were not significant.

The fabricated chip was evaluated with the aid of a gamma radiation facility capable of providing a high dose rate of up to 1 Mrad/h (Si) from a Cobalt 60 source. The gamma irradiation procedures were performed at two different total doses of 300 krad (Si) and 500 krad (Si), at the same dose rate of 100 krad/h. For each different total dose, two test chips were irradiated separately. Each fabricated n-MOSFET was irradiated under the worst bias condition, where voltages of 1.8 V, 0 V, 0 V, 0 V, and

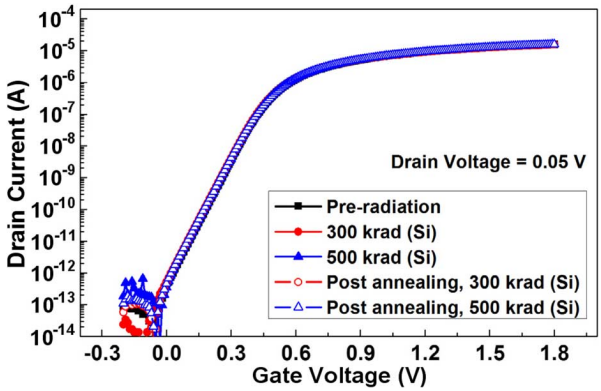

Fig. 11. Experimental results for the $V_g - I_d$ curve of the proposed n-MOSFET before and after irradiation with total doses of 300 krad (Si) and 500 krad (Si) given at the same dose rate of 100 krad/h. The measurement was taken with a drain-to-source voltage of 0.05 V; the W/L ratio of the n-MOSFETs was 1.2 μm/1.2μm.

1.8 V were applied to the gate, source, drain, body, and field Metal-1, respectively.

Moreover during the radiation exposure, a voltage of 0 V was applied to the dummy gate and dummy Metal-1 in the proposed layout, although this was not a flat band voltage. The flat band voltages of the dummy gate and dummy Metal-1 were estimated to be -0.98 V and -0.93 V, respectively. The effects of the voltages of the dummy gate and dummy Metal-1 will be investigated in a subsequent paper. In order to evaluate the applicability of the proposed layout in a commercial chip, which generally provides two voltages for the GND and VDD, a voltage of 0 V was applied to the dummy gate and dummy Metal-1 layer during the gamma radiation exposure. Moreover, although 0 V was applied to the dummy gate and dummy Metal-1 layer, it was expected that the hole trapping under each layer would be suppressed because relatively low strength electric fields were applied.

Each measurement was performed immediately after the radiation exposure and after annealing. The annealing procedure followed the ESA/SSC Basic Specification No. 22900 of 24 h at room temperature and subsequently 168 h at 100°C under the worst bias condition.

Fig. 10 presents the experimental results for the $\mathrm{V_g} - \mathrm{I_d}$ curve of the conventional n-MOSFET before and after the irradiation. After exposure to 300 krad (Si) and 500 krad (Si) of gamma radiation, the leakage currents increased significantly to 0.48 μA and 0.89 μA, respectively, at a $\mathrm{V_g}$ of 0 V. These leakage current amounts were higher than the experimental results reported for the same total dose in other research [20]. The current experimental results imply that the n-MOSFET fabricated in this study was more vulnerable to radiation conditions. Moreover, after annealing, the radiation-induced leakage currents decreased to 4.1 nA and 14.9 nA for 300 krad (Si) and 500 krad (Si) of gamma radiation, respectively, at a $\mathrm{V_g}$ of 0 V.

Comparing the experimental results and simulation results, the 300 krad (Si) of gamma radiation corresponds to a fixed charge density of 2.93×10^{12} $\#/\mathrm{cm}^2$, whereas the 500 krad (Si) of gamma radiation corresponds to a fixed charge density of 3.26×10^{12} $\#/\mathrm{cm}^2$ before annealing.

In contrast, Fig. 11 presents the experimental results for the $\mathrm{V_g} - \mathrm{I_d}$ curve of the proposed DGA n-MOSFET before and after the irradiation. The figure demonstrates that the leakage current was nearly unchanged, as expected, after exposure to 300 krad (Si) and 500 krad (Si) of gamma radiation. As with the leakage current, the on-current characteristic was practically unchanged as well. Moreover, after annealing, the leakage currents remained steady at a few hundred femto amperes.

Furthermore, the leakage current between the two transistors was measured before and after 500 krad (Si) of total dose. When the leakage currents between the two transistors were measured, the $\mathrm{n+}$ junction of one transistor was biased to 0 V and that of the other transistor was biased to 1.8 V. Moreover, the field Metal-1 layer, which overlaps each $\mathrm{n+}$ junction, between the two transistors was swept from 0 V to 65 V. The transistor, in which the field Metal-1 layer functions as a transistor gate, was named as a field Metal-1 transistor. The field Metal-1 transistor had a very high threshold voltage of approximately 65 V because the gate oxide was very thick. The threshold voltage of the field Metal-1 transistor between the two conventional n-MOSFETs was shifted by approximately 15 V after exposure to 500 krad (Si) of gamma radiation. However, the threshold voltage of the field Metal-1 transistor between the two DGA n-MOSFETs was not shifted. Nevertheless, at the field Metal-1 layer voltage of 1.8 V, the leakage current maintained a few hundred femto amperes in both the conventional n-MOSFETs and the proposed DGA n-MOSFETs after exposure to 500 krad (Si) of gamma radiation. These results imply that the chip, fabricated using MagnaChip & Hynix 0.18 $\mu\mathrm{m}$ technology, has radiation-tolerant characteristics regarding leakage currents between two transistors up to 500 krad (Si) of total dose.

V. Conclusion

A new radiation-tolerant n-MOSFET layout termed a DGA n-MOSFET layout was evaluated for a radiation-tolerant circuit design. For practical purposes, the proposed DGA n-MOSFET layout does not have limitations with regard to the W/L ratio and asymmetrical geometry. Furthermore, compared with the ELT, it has a relatively smaller gate capacitance and smaller footprint. Therefore, the design limitations with regard to the limited W/L ratio in analog circuit design and the operating speed limitation with regard to the larger gate capacitance in the digital circuit design can be supplemented. Nevertheless, the proposed DGA n-MOSFET results in a slight operating speed degradation in the digital circuit compared with the conventional n-MOSFET.

The proposed DGA n-MOSFET layout eliminated all radiation-induced leakage current paths by isolating both the source and drain from the sidewall oxides using a $\mathrm{p+}$ layer and dummy gates. The simulation results demonstrate that the proposed DGA n-MOSFET structure performed well, as expected, even though the fixed charge density increased. Furthermore, from the experimental results, the fabricated DGA n-MOSFET exhibited good performance, even after exposure to 500 krad (Si) of gamma radiation. The experimental results confirm that the proposed DGA n-MOSFET layout is adequate for radiation-tolerant electronic devices, even when a voltage of 0 V is applied to both the dummy gates and dummy Metal-1 layer.

Acknowledgment

The authors would like to thank Dr. N. H. Lee and Dr. H. J. Lee at the Korea Atomic Energy Research Institute, as well as Dr. K. S. Ryu from the Satellite Technology Research Center at Korea Advanced Institute of Science and Technology for their helpful comments.