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Characterization of interface trap dynamics responsible for hysteresis in organic thin-film transistors

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ABSTRACT

In this paper, the current hysteresis of organic thin film transistors (OTFTs) formed by TIPS-Pentacene has been demonstrated by bi-directional gate-voltage scan and explained using the trapping and detrapping mechanism. The trapping and detrapping rates have been further verified by the gate-voltage sampling method and the channel charge pumping method. The validity of the methods to characterize interface states of OTFTs that lead to the hysteresis is justified. The two independent methods consistently reveal that the hole trapping and release rates at the interface between the channel of the OTFTs to the gate dielectric are asymmetric.

1. Introduction

Organic thin film transistors (OTFTs) have been widely investigated due to their potential for low cost and large area electronic applications [1,2] such as e-paper displays, low-end RFID card [3] and chemical/biology sensors [4]. One major problem of OTFTs is the operational instability, including the short term hysteresis and long term permanent degradation [5–10]. The hysteresis in OTFTs transfer characteristics have been widely studied in the literature and several physical theories have been proposed [11], including the trapped charges near the channel/dielectric interface, mobile ions or polarization in the dielectric, and charge injection from the gate to the dielectric [12,13]. Further refinement of the trapped charge mechanism has resulted in the minority and majority trap theory [14,15]. The minority trap theory has gained wider acceptance with the demonstration of the hydroxyl group and the H_2O/O_2 redox couple near the dielectric/channel interface acting as electron traps [16,17]. According to the trapped charge theory, trapped electrons by the hydroxyl group or the H_2O/O_2 redox couple near interfaces of the dielectric are neutralized by the majority holes leading to a change in the device threshold voltage during gate voltage sweeping [18,19]. Even though the chemical nature of the above two mechanisms is different, the electrical behavior (hysteresis) is the same. Most of the published characterization works focus on interface defects density with some individual hole trapping time measurement using the constant gate-voltage sampling method [20,21]. It is true that the gate-voltage sampling method has been used to obtain the trapping rate, but it has not been used to measure the detrapping process to give a full picture of the hysteresis phenomenon. In addition, the accuracy of the method has not been compared with other existing techniques.

In this work, the trapping process for TIPS-Pentacene OTFT is first studied using the gate-voltage sampling method. The channel charge pumping method is applied as an independent technique to verify the result. Then the detrapping process is characterized using the same two techniques. The detrapping process during the measurement is explained and the relevant equations are derived. With the same techniques and a different set of equations, the detrapping time is extracted. We use the terms of trapping and detrapping processes to represent the behavior of holes in p-type OTFT, i.e. the interface negative charge neutralization is described as hole trapping while the negative charge re-emergence is described as hole releasing.

2. Device structure and bi-directional gate sweeping measurement

Generic bottom-gate/bottom-contact thin film transistors as sketched in Fig. 1 are prepared from the drop casting process with

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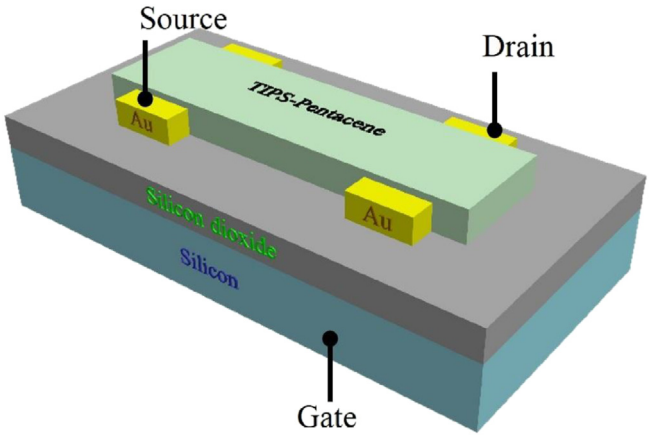

Fig. 1. Bottom gate/bottom contact OTFT configuration.

TIPS-Pentacene as the channel material. The bottom gate electrode is composed of p-type silicon substrate. 100 nm silicon dioxide (SiO_2) is thermally grown as the gate dielectric. Au/Ti (100 nm/5 nm) electrodes are evaporated on the SiO_2 and patterned using the lift off process to form the source/drain terminals. The active region is formed from a solution prepared by dissolving TIPS-Pentacene in toluene with a 0.6% wt. Control metal/oxide/silicon capacitors without organic material are also fabricated using the same process. The capacitance–voltage measurements of the control devices do not show any hysteresis. This fact eliminates the possibility of mobile ions inside the silicon dioxide.

The gate voltage (V_g) ramped from zero to a minimum voltage and back to zero is represented by a stair waveform where the width of the step represents the integration time during measurement. The drain voltage (V_d) is kept at −30 V and the drain current is measured using the parametric analyzer Agilent 4156C. The measured drain current (I_d) with an average ramp rate of 1.7 V/s is plotted in Fig. 2(a). The drain current measured during the negative sweep is observed to be smaller than that measured during the positive sweep. The hysteresis behavior is stable and repeatable with consecutive gate-voltage sweeps.

Using the trapping/detrapping theory, the hysteresis can be explained by the slow trapping rate and fast detrapping rate. To verify that the asymmetric trapping and detrapping rates are indeed the cause of the hysteresis, different sweep rates are applied to the transistors. When the sweep rate is increased to 5.2 V/s, the hysteresis almost disappears. This is because at a sweep rate faster than both the charging and discharging process, the interface traps cannot respond and remain in the same initial state leading to identical currents in both sweep directions. When the sweep rate is significantly reduced to 0.1 V/s with a 0.2 s integration time which is slower than both the trapping and detrapping rates, equilibrium can be achieved in both sweeping directions and leads to smaller hysteresis. The measurement results agree with the prediction from the trapping/detrapping theory.

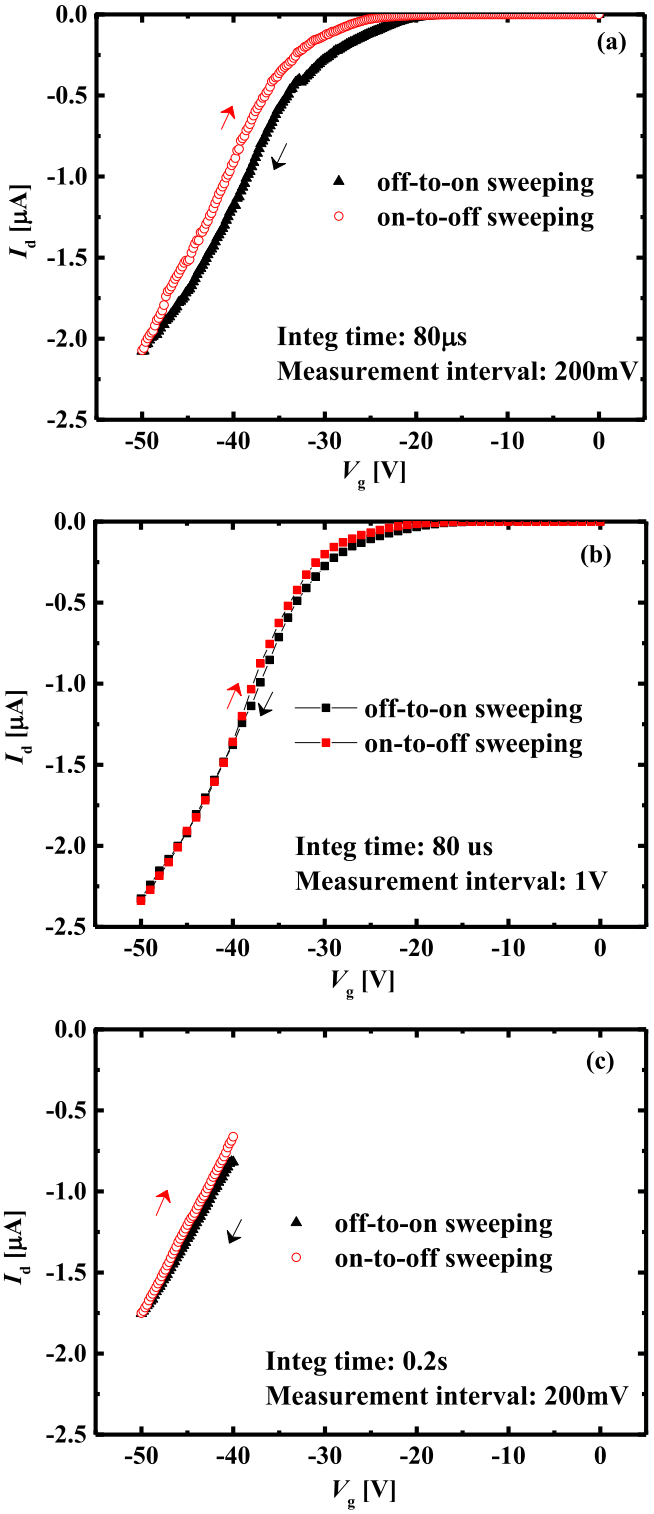

Fig. 2. I_d–V_g double sweeping at (a) intermediate sweep rate; (b) fast sweep rate; (c) slow sweep rate from −40 to −50 to −40 V.

3. Determining the charge trapping rate

To establish the validity of the widely applied gate-voltage sampling method and determine the charge trapping rate, the result of the gate-voltage sampling method is compared with that of the channel charge pumping method. The setup of the gate-voltage sampling method is shown in the inset of Fig. 3(a). Different gate voltages of −40 V, −35 V and −30 V are applied to the gate and kept constant throughout the measurement. With the extracted threshold voltage from the fast gate sweep measurement as −15 V, a high constant voltage of −30 V is applied to the drain to give the saturation current. In this situation, the interface traps are continuingly filled by the charges from the source. When all the traps are occupied, the drain current decreases to a constant value.

The characterized trapping behavior is reversible and

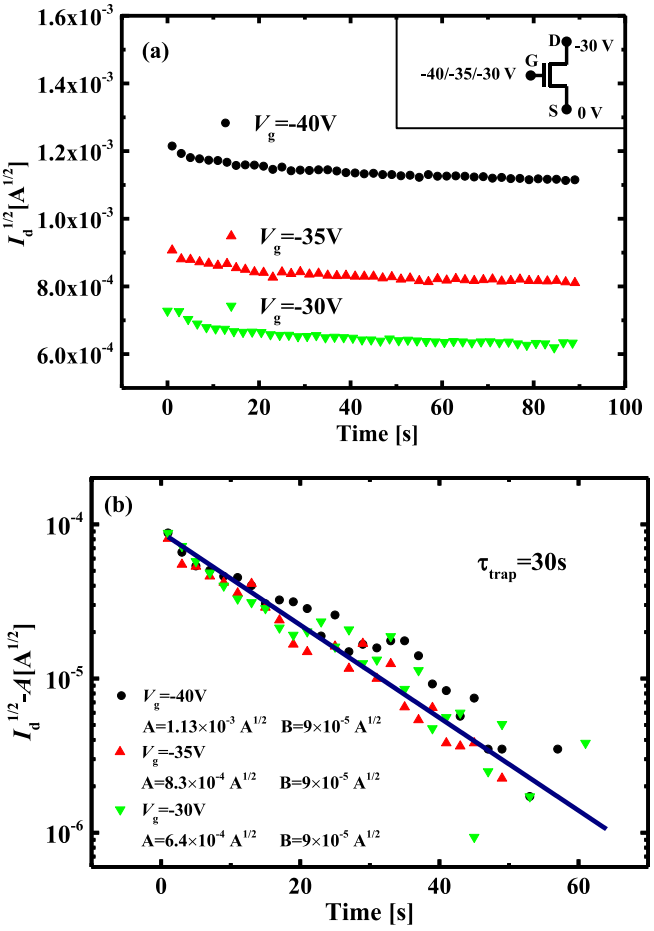

Fig. 3. (a) Measured square root of saturation current (solid points). Inset: measurement setup (b) log ($\sqrt{I_d} - A$) versus time. Measured data (solid points), fitting data (solid line).

repeatable. For this short term reversible trapping behavior that does not involve metastable state creation [22], the rate of trap filling can be given by Refs. [23,24].

$$d\Delta N/dt = (N_{\text{tot}} - \Delta N)/\tau_{\text{trap}} \tag{1}$$

where N_{tot} is the total density of interface states, ΔN is the density of filled states and τ_{trap} is the trapping rate. The differential equation can be solved assuming the initial condition that ΔN equals to zero at $t = 0$ yielding

$$\Delta N = N_{\text{tot}}[1 - \exp(-t/\tau_{\text{trap}})] \tag{2}$$

The change of interface state density can be described in terms of threshold voltage V_{th} shift as in

$$\Delta V_{\text{th}} = V_{\text{th}} - V_{\text{th0}} = q\Delta N/C_{\text{ox}} \tag{3}$$

where V_{th0} is the initial threshold voltage and C_{ox} is the gate capacitor. As a result, the time dependent threshold voltage is derived by combining Eqs. (2) and (3), which gives

$$V_{\text{th}} = V_{\text{th0}} + (qN_{\text{tot}}/C_{\text{ox}}) \cdot [1 - \exp(-t/\tau_{\text{trap}})] \tag{4}$$

The conventional saturation drain current equation provides the relationship between the drain current and the threshold voltage which is given by

$$I_{\text{d}} = (1/2)\mu(W/L)C_{\text{ox}}(V_{\text{g}} - V_{\text{th}})^2 \tag{5}$$

where μ is carrier mobility, and W/L is the device width/length. Combining Eqs. (4) and (5), the time constant can be extracted from the exponential change of the square root of saturation current which gives

$$\begin{aligned}\sqrt{I_d} &= \sqrt{(1/2)\mu(W/L)C_{ox}}(V_g - V_{th0} - qN_{tot}/C_{ox} \\ &\quad + (qN_{tot}/C_{ox}) \cdot \exp(-t/\tau_{trap})) \\ &= A + B \cdot \exp(-t/\tau_{trap})\end{aligned} \tag{6}$$

where $A = \sqrt{k}(V_g - V_{th0} - q/C_{ox})$, $B = \sqrt{k}(qN_{\text{tot}}/C_{ox})$ and $k = (1/2)\mu(W/L)C_{ox}$. Under different gate biases, the interface trap density should be the same. This can be extracted from the total $\sqrt{I_d}$ change after around 90 s when almost all the traps are occupied by holes. With the initial value of $\sqrt{I_d}$ at $t = 0$ s, the value of A under various gate voltages is obtained. On the basis of equation (6), plotting log ($\sqrt{I_d} - A$) versus time is supposed to provide a straight line with a slope equal to $1/\tau_{\text{trap}}$. The log ($\sqrt{I_d} - A$) versus time plot is given in Fig. 3(b). Using least square fitting, the trapping rate is estimated to be around 30 s. The interface trap density extracted from $\sqrt{I_d}$ change is about 3.5 × 10^{13} cm^{-2}. The obtained trapping time is consistent with the reported data in Ref. [14] and [25]. The extracted interface trap density is in the range of the typical value of OTFTs with SiO_2 dielectric, which are in the order of 10^{11} cm^{-2} to 10^{13} cm^{-2} [26,27].

In addition to the gate-voltage sampling method, the channel charge pumping method [28] is used as an independent method to confirm the experimental result. The setup of the channel charge pumping measurement is illustrated in the inset of Fig. 4 with a pulse signal applied to the gate of the OTFT and with the drain voltage fixed at 0 V. Under such condition, there is no DC current from the source to drain and the measured drain current only consists of the transient channel and trap charging/discharging currents. The transient drain current is sampled at a rate of 25 Points/s to capture the dynamics of the response. At the falling edge of the pulse, the channel is turned on and holes enter the channel resulting a transient drain current. When the pulse is leveled out at −40 V, the channel charging current stops. However, the interface trapping rate is relatively slow and the charge trapping current

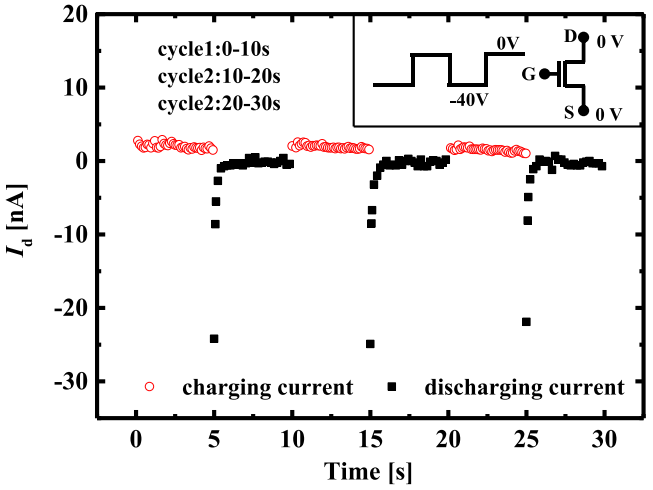

Fig. 4. Charging (hollow red circle) and discharging (solid black square) current. Inset: measurement setup. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

continues to flow as shown in the hollow circle in Fig. 4. As the number of unfilled traps decreases with time, the drain current gradually returns to zero when all the traps are filled.

The channel charging current is then given by

$$I_{\text{charge}} = qd\Delta N/dt = \left(qN_{\text{tot}}/\tau_{\text{trap}}\right)\cdot\exp\left(-t/\tau_{\text{trap}}\right) = 2I_{\text{d}} \quad (7)$$

The total drain current needs to be multiplied by 2 due to the symmetrical configuration between the source and drain. According to equation (7), plotting log (I_{d}) versus time is expected to give a straight line with a slope equal to $1/\tau_{\text{trap}}$. The log (I_{d}) versus time plot is given in Fig. 5. Despite of some random fluctuation, the overall trend more or less follows a straight line. Using the least square estimation, the best linear fitting function and experimental data are shown in Fig. 5. From the slope and the intercept of Fig. 5, we have extracted the trapping rate to be 30 s and the total number of traps at the interface is 3.1×10^{13} cm^{-2}, which is very close to the value obtained from the gate-voltage sampling measurement. The consistency of the two independent methods justifies the accuracy of the technique.

4. Determining the charge detrapping rate

The gate-voltage sampling method can also be used to determine the charge detrapping rate and the result is further verified by the channel charge pumping method. The setup of the gate-voltage sampling measurement is shown in the inset of Fig. 6(a). Different voltages of −40 V, −35 V and −30 V are applied to the gate. The transient recovery current is measured when the gate is switched off. With the applied drain voltage returning to zero, the channel charge is swept back to the drain terminal instead of both the source and drain electrodes. The slow detrapping of the interface states gives a continuous current tail as shown in Fig 6(a). To capture the transient current, a sampling rate at 50 points per second is used.

The detrapping process is governed by the following equation with τ_{detrap} as detrapping rate:

$$d\Delta N/dt = -\Delta N\Big/\tau_{\text{detrap}} \quad (8)$$

Assuming the states are completely filled at the beginning of the process, ΔN is given by:

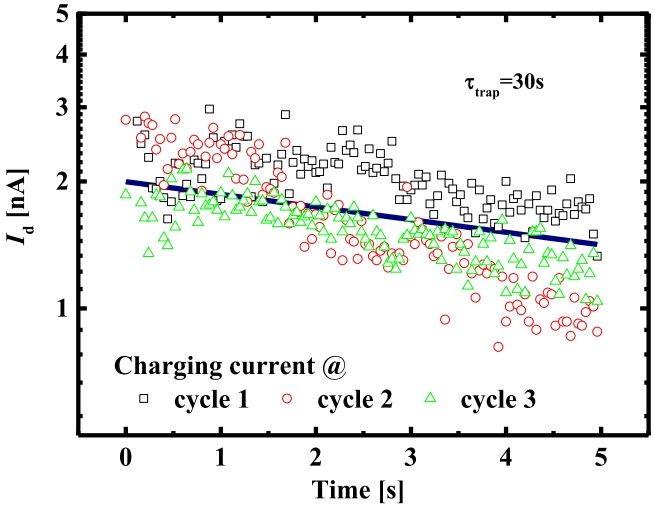

Fig. 5. Measured I_{d} (hollow symbols) and the best linear fit (navy solid line). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

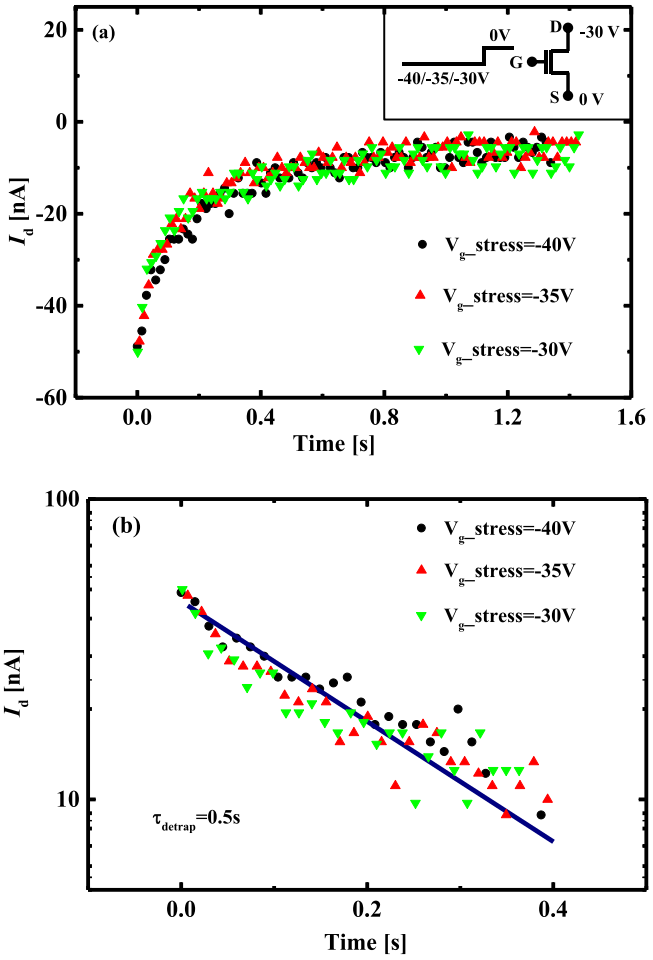

Fig. 6. (a) Measured discharging current (solid points). Inset: measurement setup (b) log (I_{d}) versus time. Measured data (solid points), fitting data (solid line).

$$\Delta N = N_{\text{tot}}\exp\left(-t\Big/\tau_{\text{detrap}}\right) \quad (9)$$

The detrapping current can then be expressed as:

$$I_{\text{discharge}} = qd\Delta N/dt = -\left(qN_{\text{tot}}\Big/\tau_{\text{detrap}}\right)\cdot\exp\left(-t\Big/\tau_{\text{detrap}}\right) = I_{\text{d}} \quad (10)$$

Similar recovery behaviors are expected under different voltages since the detrapping process should be irrelevant to the historical stress. To extract the detrapping rate, log (I_{d}) is plotted versus time as shown in Fig. 6(b). Applying least square fitting, the detrapping rate is estimated to be around 0.5 s. The total number of traps at the interface extracted from the intercept of the fitted curve is about 3.2×10^{13} cm^{-2}.

Besides the gate-voltage sampling method, the channel charge pumping method is used as a separate method to support the experimental result. In the case of channel charge pumping measurement, the detrapping rate is determined by observing the drain current when the gate voltage returns to zero from −40 V, which is indicated by the solid square in Fig. 4. When the channel is turned off by the gate voltage, the channel charge is driven back to the source/drain leading to a very quick negative transient spike. When the channel is fully discharged, the current returns to zero. However, the detrapping of the interface states is much slower than the discharging of the channel charge, leading to a continuous current

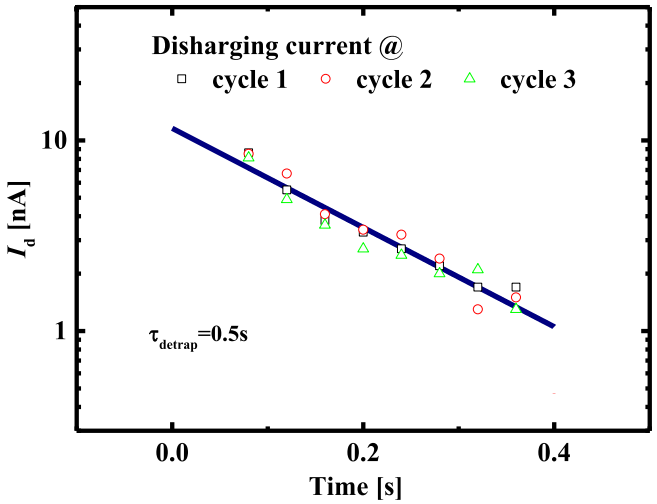

Fig. 7. Measured discharging current (hollow symbols) and the best linear fit (navy solid line). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

tail flowing to the source and drain due to the release of holes. The detrapping process is governed by the equations (8)–(9) which results in

$$I_{\text{discharge}} = qd\Delta N/dt = -\left(qN_{\text{tot}}\Big/\tau_{\text{detrap}}\right)\cdot\exp\left(-t\Big/\tau_{\text{detrap}}\right) = 2I_{\text{d}} \tag{11}$$

which is the same as equation (10) except that the discharging current flows to both the source and drain sides.

As shown in Fig. 4, the detrapping rate is much faster than the trapping rate and the transient current is sampled at a rate of 25 samples per second to capture the detailed waveform. To extract the detrapping rate, log (I_d) is plotted versus time, as shown in Fig. 7, at different cycles of the clock to check for consistency. The trend also follows a straight line which shows that the theory is reasonable. Using least square fitting, the detrapping rate is estimated to be around 0.5 s. The obtained total number of traps at the interface from the intercept of the fitted curve is about 2.9×10^{13} cm^{-2}. The validity of the gate-voltage sampling method for detrapping time extraction is confirmed by the consistent result of the channel charge pumping method.

5. Conclusion

In this paper, the gate-voltage sampling method is applied to extract both the trapping and detrapping rates. The detrapping process during the measurement is explained and the relevant equations are derived. The estimated trapping rate is around 30 s while the detrapping rate is about 0.5 s. To verify the validity of the technique, the channel charge pumping method is used. Since in the trapping and detrapping process the total trap densities measured using both methods are consistent with each other, giving a value close to 3.2×10^{13} cm^{-2}, the accuracy of the technique is confirmed.

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References

[1] A.C. Arias, J.D. MacKenzie, I. McCulloch, et al., Materials and applications for large area electronics: solution-based approaches, Chem. Rev. 110 (1) (2010) 3–24.
[2] Z. Bao, Materials and fabrication needs for low-cost organic transistor circuits, Adv. Mater. 12 (3) (2000) 227–230.
[3] R. Rotzoll, S. Mohapatra, V. Olariu, et al., Radio frequency rectifiers based on organic thin-film transistors, Appl. Phys. Lett. 88 (12) (2006) 123502–123502-3.
[4] H.U. Khan, M.E. Roberts, W. Knoll, et al., Pentacene based organic thin film transistors as the transducer for biochemical sensing in aqueous media, Chem. Mater. 23 (7) (2011) 1946–1953.
[5] G. Gu, M.G. Kane, J.E. Doty, et al., Electron traps and hysteresis in pentacene-based organic thin-film transistors, Appl. Phys. Lett. 87 (24) (2005) 243512–243512-3.
[6] C.S. Kim, S. Lee, E.D. Gomez, et al., Solvent-dependent electrical characteristics and stability of organic thin-film transistors with drop cast bis (triisopropylsilylethynyl) pentacene, Appl. Phys. Lett. 93 (10) (2008) 103302.
[7] S.K. Park, D.A. Mourey, J.I. Han, et al., Environmental and operational stability of solution-processed 6, 13-bis (triisopropyl-silylethynyl) pentacene thin film transistors, Org. Electron. 10 (3) (2009) 486–490.
[8] B. Lee, A. Wan, D. Mastrogiovanni, et al., Origin of the bias stress instability in single-crystal organic field-effect transistors, Phys. Rev. B 82 (8) (2010) 085302.
[9] N. Padma, V. Saxena, V. Sudarsan, et al., Disordered Self assembled monolayer dielectric induced hysteresis in organic field effect transistors, J. Nanosci. Nanotechnol. 14 (6) (2014) 4418–4423.
[10] C. Liu, Y. Xu, Y. Li, et al., Critical impact of gate dielectric interfaces on the contact resistance of high-performance organic field-effect transistors, J. Phys. Chem. C 117 (23) (2013) 12337–12345.
[11] M. Egginger, S. Bauer, R. Schwödiauer, et al., Current versus gate voltage hysteresis in organic field effect transistors, Monatsh. Chemie-Chemical Mon. 140 (7) (2009) 735–750.
[12] G. Gu, M.G. Kane, J.E. Doty, et al., Electron traps and hysteresis in pentacene-based organic thin-film transistors, Appl. Phys. Lett. 87 (24) (2005) 243512–243512-3.
[13] D.K. Hwang, M.S. Oh, J.M. Hwang, et al., Hysteresis mechanisms of pentacene thin-film transistors with polymer/oxide bilayer gate dielectrics, Appl. Phys. Lett. 92 (1) (2008) 013304.
[14] G. Gu, M.G. Kane, S.C. Mau, Reversible memory effects and acceptor states in pentacene-based organic thin-film transistors, J. Appl. Phys. 101 (1) (2007) 014504.
[15] C. Ucurum, H. Goebel, F.A. Yildirim, et al., Hole trap related hysteresis in pentacene field-effect transistors, J. Appl. Phys. 104 (8) (2008) 084501–084501-5.
[16] M. Qu, H. Li, R. Liu, et al., Interaction of bipolaron with the H_2O/O_2 redox couple causes current hysteresis in organic thin-film transistors, Nat. Commun. 5 (2014).
[17] L.L. Chua, J. Zaumseil, J.F. Chang, et al., General observation of n-type field-effect behaviour in organic semiconductors, Nature 434 (7030) (2005) 194–199.
[18] C.M. Aguirre, P.L. Levesque, M. Paillet, et al., The role of the oxygen/water redox couple in suppressing electron conduction in field-effect transistors, Adv. Mater. 21 (30) (2009) 3087–3091.
[19] S. Lee, B. Koo, J. Shin, et al., Effects of hydroxyl groups in polymeric dielectrics on organic transistor performance, Appl. Phys. Lett. 88 (16) (2006) 162109.
[20] K.K. Ryu, I. Nausieda, D.D. He, et al., Bias-stress effect in pentacene organic thin-film transistors, Electron Devices IEEE Trans. 57 (5) (2010) 1003–1008.
[21] P.A. Bobbert, A. Sharma, S.G.J. Mathijssen, et al., Operational stability of organic field-effect transistors, Adv. Mater. 24 (9) (2012) 1146–1158.
[22] M.J. Powell, C. Van Berkel, J.R. Hughes, Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors, Appl. Phys. Lett. 54 (14) (1989) 1323–1325.
[23] C. Ma, H. Mattausch, M. Miura-Mattausch, et al., Universal NBTI compact model for circuit aging simulation under any stress conditions, IEEE Trans. Device Mater. Reliab. 14 (3) (2014) 818–825.
[24] S. Mahapatra, K. Ahmed, D. Varghese, et al., On the physical mechanism of NBTI in silicon oxynitride p-MOSFETs, in: Can Differences in Insulator Processing Conditions Resolve the Interface Trap Generation versus Hole Trapping Controversy? Reliability Physics Symposium, 2007. Proceedings. 45th Annual. IEEE International. IEEE, 2007, pp. 1–9.
[25] A. Salleo, F. Endicott, R.A. Street, Reversible and irreversible trapping at room temperature in poly (thiophene) thin-film transistors, Appl. Phys. Lett. 86 (26) (2005) 263505.
[26] S. Lee, S.J. Kang, G. Jo, et al., Enhanced characteristics of pentacene field-effect transistors with graphene electrodes and substrate treatments, Appl. Phys. Lett. 99 (8) (2011) 083306.
[27] G. Horowitz, M.E. Hajlaoui, R. Hajlaoui, Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors, J. Appl. Phys. 87 (9) (2000) 4456–4463.
[28] M. Koyanagi, I.W. Wu, A.G. Lewis, et al., Evaluation of polycrystalline silicon thin film transistors with the charge pumping technique, in: Electron Devices Meeting, 1990. IEDM'90. Technical Digest., International. IEEE, 1990, pp. 863–866.