Investigation of Anti-Islanding Protection of Power Converter Based Distributed Generators Using Frequency Domain Analysis

Vinod John, *Member, IEEE*, Zhihong Ye, *Member, IEEE*, and Amol Kolwalkar, *Member, IEEE*

***Abstract*—The anti-islanding algorithm proposed by the Sandia National Laboratories is analyzed in this study because this scheme, also known as the Sandia scheme, is considered to be effective in detecting islanding of distributed generation systems. Previously, other than heuristic approaches, there has not been any quantitative analysis for tuning the control gains of the algorithm based on the power rating and bandwidth of the distributed generation (DG) power converter. The paper interprets the components of the algorithm that affect the voltage magnitude and frequency into block diagrams that can be linearized and studied using continuous time approximations. This paper uses frequency domain approach to analyze the range for the gains required by anti-islanding algorithm to effectively determine the disconnection of the mains grid within an acceptable time duration. The analysis provides guidelines for using the Sandia's schemes under different application conditions. The results are validated using detailed time domain DG and power system simulations.**

***Index Terms*—Anti-islanding, distributed generation (DG), inverters, power conditioning, power system protection, power system simulation, power system state estimation, Sandia frequency scheme, Sandia voltage scheme.**

I. Introduction

ISLANDING of a grid connected distributed generation (DG) occurs when a section of the utility system containing such generators is disconnected from the main utility, but the independent DGs continue to energize the utility lines in the isolated section (termed as an island). Unintended islanding is a concern primarily because it poses a hazard to utility and customer equipment, maintenance personnel, and the general public. Poor power quality can damage loads in the island. Another concern is the out of phase switching of reclosers leading to damage to the DG, neighboring loads, and utility equipment.

Many techniques have been proposed to prevent islanding caused by DGs [1]–[9]. An algorithm proposed by the Sandia National Laboratories is analyzed in this study because it is considered to be effective in detecting the formation of such islands [1], [4]. Sandia's active islanding algorithms had been developed for single-phase inverter units. The algorithm consists of the Sandia frequency shift (SFS) and the Sandia voltage shift (SVS) schemes. The principle behind both the methods is an accelerated frequency and voltage drift created with positive feedback. In the presence of the utility, the frequency and voltage shifts are not effective in drifting the two parameters. However, once the grid is disconnected, these methods force the frequency and/or voltage to shift outside the operating windows, causing the inverter to disconnect due to o/u voltage and frequency protection.

Since these were originally developed for a single-phase inverter, the technique adopted to measure frequency is based on the zero crossing of the voltage waveform, and the voltage magnitude is obtained from RMS calculations. This method has been extended to three phase DGs that utilize three-phase continuous tracking phase locked loop (PLL) in a synchronous reference frame [10].

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V. John is with Northern Power Systems, Waitsfield, VT 05602 USA.

Z. Ye is with General Electric Corporate Research and Development, Niskayuna, NY 12309 USA (e-mail: ye@crd.ge.com).

A. Kolwalkar is with General Electric Global Research Center, Bangalore 560 066, India.

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II. Analysis of Sandia Anti-Islanding Algorithm

Implementation of the Sandia anti-islanding algorithm is described in [1]. However, a systematic approach to tuning these algorithms has not been described in literature before. The parameters design is mostly performed on a heuristic basis to date.

A block diagram interpretation of the Sandia's algorithm is shown in Fig. 1. This block diagram model of the anti-islanding algorithms is to determine the gain settings for the SVS and the SFS algorithms. The critical gains of the Sandia anti-islanding algorithm are

- K_f for the SFS;
- K_{vp} and K_v for SVS;
- ω_{f1} for the wash out functions;
- ω_{f2} for the real and reactive power regulation loop.

The critical gains for SFS and SVS have to be determined for resistance–inductance–capacitance (RLC) loads (set according to IEEE 1547) so as to mitigate islanding situations [11]. The gain settings of the algorithm, shown in Fig. 1, have been obtained by performing a small signal analysis of the DG system with the tuned RLC load (according to IEEE 929–2000 and UL 1741 anti-islanding test specifications) [12], [13].

The basic principle of the algorithms can be described as follows.

For SVS, the inverter terminal voltage variation can be obtained by the washout function. Then after gains K_v and $P*K_{\mathrm{vp}}$, a power variation is obtained and add onto the original power reference. After divided by the voltage magnitude, the current reference magnitude $\mathrm{Id}*$ is obtained to generate inverter

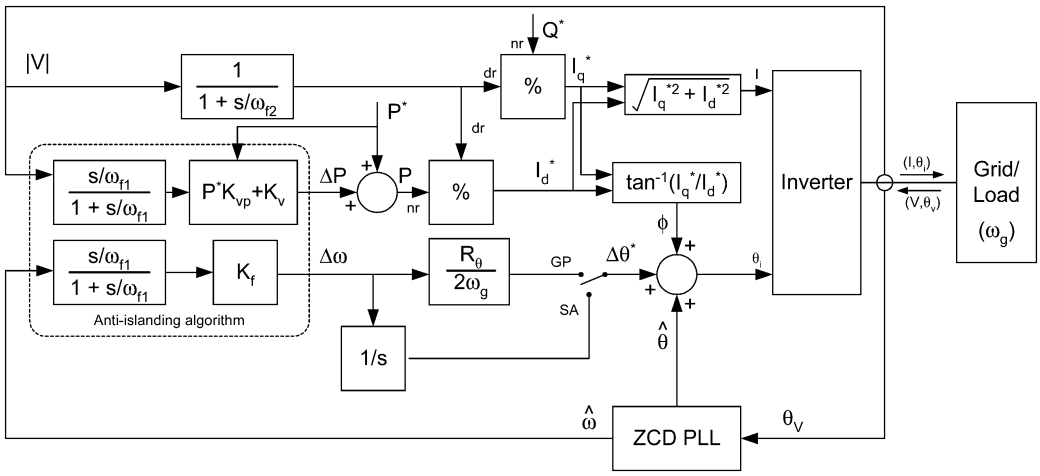

Fig. 1. Block diagram representation of the Sandia's anti-islanding algorithm.

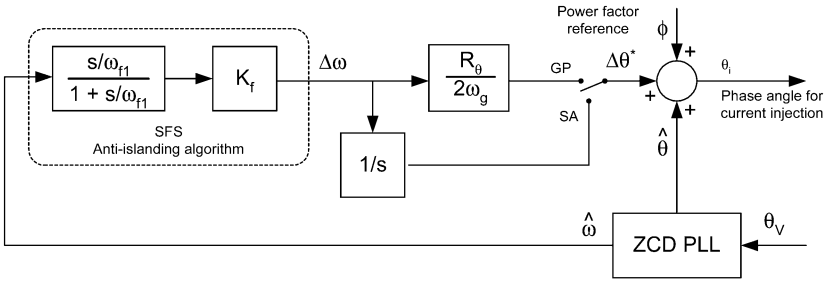

Fig. 2. Block diagram highlighting the SFS component of the Sandia's anti-islanding algorithm.

current magnitude reference. There is a positive feedback loop in that when voltage becomes higher, the current reference will become higher and causes the voltage even higher. Consequently over voltage relay will trip to protect the system from a sustained islanding situation. This loop, however, is only dominantly effective when islanded. When grid connected, the loop has minimal effect on the voltage since the grid is regulating the voltage. A similar control philosophy applies to SFS. The SVS modifies DG power reference based on measured voltage magnitude and the SFS modified current phase angle based on measured frequency. Hence, these schemes act differently compared to traditional power system exciter and governor functions.

The algorithm gains are determined by investigating the open loop behavior as a function of frequency. The voltage magnitude and the phase signal flow paths were opened so as to obtain the SVS and SFS gains, respectively. The Sandia voltage and frequency schemes and the derivation of the block diagram representations are explained in detail as follows.

A. SFS Algorithm

The block diagram of the SFS algorithm is shown in Fig. 2. The frequency estimate from the PLL is passed through a washout function to determine changes in the ambient frequency. This information multiplied by the SFS gain, is added to the frequency reference of the current injected by the DG inverter. As the DG commanded frequency on average cannot be different from the grid frequency, the phase angle has to be periodically reset for meaningful power transfer from the DG to the rest of the grid system to occur. In the single-phase

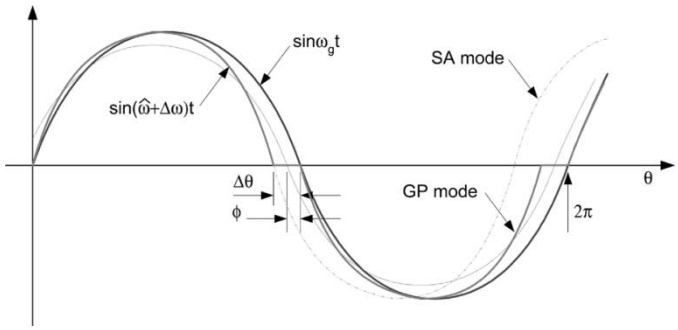

Fig. 3. Nature of waveforms caused by the SFS algorithm.

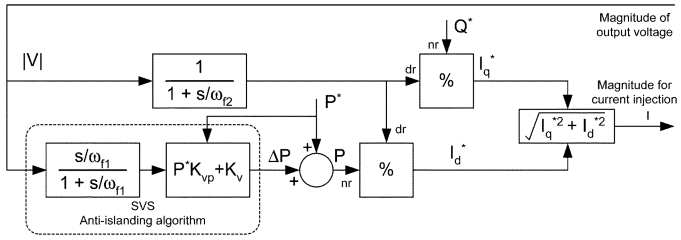

Fig. 4. Block diagram highlighting the SVS component of the Sandia's anti-islanding algorithm.

case, this reset of the phase angle in the DG current reference waveform occurs at the voltage zero crossings.

In grid parallel mode (GP), the grid sets the frequency of operation of the DG. The $R_\theta/2\omega_g$ block in Fig. 2 is an equivalent representation of the actual DG system behavior that captures the change in the phase corresponding to the error in frequency. The derivation of this block in the GP is based on the equivalent phase

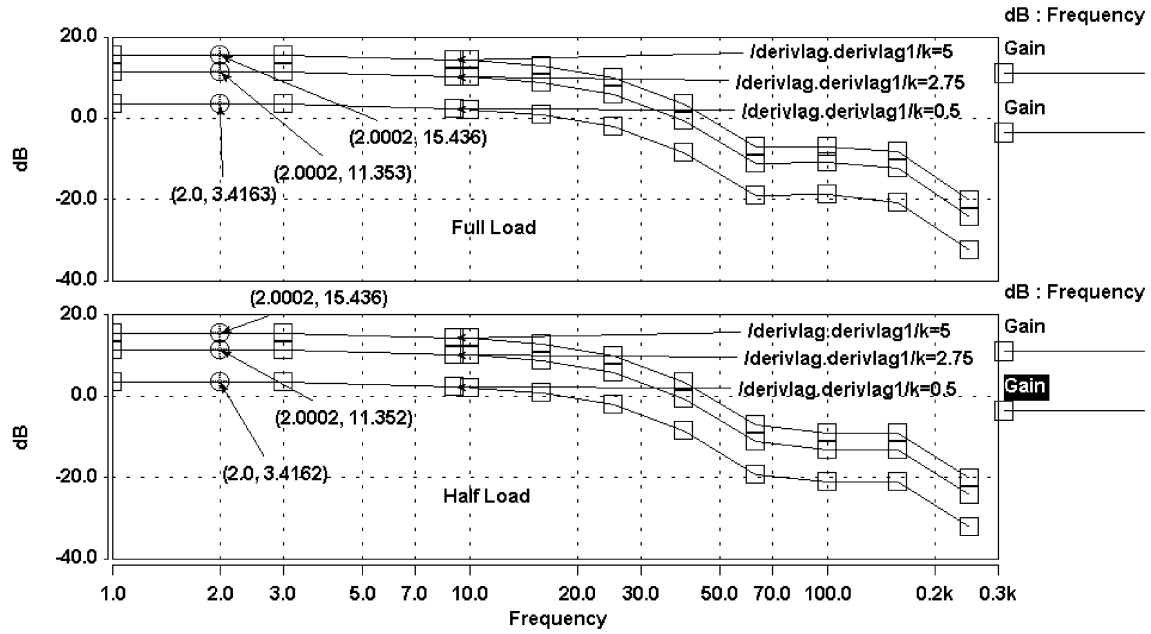

Fig. 5. Loop gain (in decibals) of the SFS algorithm with RLC load at (top) 50% and (bottom) 100% power level between 1 and 300 Hz.

angle change (ϕ) calculated in response to a change in frequency $(\Delta\omega)$ as a function of the system frequency (ω_g). This can be explained by considering the single-phase implementation where the frequency command from the SFS is higher than the nominal frequency and reset period of 180°, as shown in Fig. 3

$$\Delta\theta = \frac{\Delta\omega T}{\frac{2\pi}{R_\theta}} \tag{1}$$

where T is the period and R_θ is the reset angle. Simplifying for the period in terms of ω_g, we get

$$\Delta\theta = \frac{\Delta\omega R_\theta}{\omega_g}. \tag{2}$$

The effective phase shift $\phi = \Delta\theta/2$. For the situation of π radians for R_θ, the phase shift is given by

$$\phi = \frac{\Delta\omega\pi}{2\omega_g} \tag{3}$$

at 60 Hz the relationship is $\phi = 4.1666e - 3\Delta\omega$.

In standalone mode (SA), the frequency of the island is set by the interaction of the DG and the load. Hence, in the SA mode, the phase angle error $(\Delta\theta*)$ caused by SFS is represented by the integral of the frequency error. This can be observed from the waveforms of the SFS algorithm shown in Fig. 3. This $\Delta\theta*$ is then added to the reference phase angle, and the power factor angle reference, to provide the reference command for the phase angle of the current injected by the DG. The magnitude of the DG current is determined by the SVS loop, as explained below. Note that the SA mode considered in this analysis is during the transition of from grid parallel mode. In this condition the grid has been disconnected but the DG has not yet made any decision for mode transition and continues to inject current out of its terminals without consideration for instantaneous DG terminal voltage regulation.

B. SVS Algorithm

The block diagram of the SVS algorithm is shown in Fig. 4. The input to this block is the magnitude of the system voltage. The error in the system voltage determines the shift in the reference power, to drive the DG voltage further away from the operating voltage range. The voltage magnitude, after a low pass filter, is also used to determine the magnitude of the reference current settings for the DG. This is to ensure that the desired level of real and reactive power is being delivered by the DG. As compared to the SFS, the gain in the feedback loop is not a constant, but is a function of the real power reference setting.

The anti-islanding algorithm works by forcing the island with the DG to become unstable whenever the grid is disconnected. Hence, for the active anti-islanding to be effective, the open loop gain has to be greater than one. The Section II-C interprets the characteristics of the SFS and SVS active anti-islanding algorithms based on frequency domain analysis.

C. Implications of the Gains Settings of the Sandia Anti-Islanding Algorithm

The analysis of block diagram representation of the anti-islanding algorithm can be used to evaluate the dependence of the gain settings of the SFS and SVS on various types of loads. The gains should be designed for the worst-case load for the schemes to be effective under all circumstances. The RLC load has a quality factor of 2.5 as defined in IEEE 929 [12] and UL 1741 [13] testing requirements. The SFS and SVS algorithms are analyzed separately assuming that they are decoupled with respect to each other. The voltage magnitude fed back into SVS is held at the nominal value during the study of SFS algorithms. The frequency measurement into SFS is held at the nominal value (60 Hz) during the analysis of the SVS algorithm.

Fig. 5 shows the open loop gain frequency response of the SFS algorithm with the RLC load at 50% and 100% power level for three different values of K_f. The plot shows the open loop

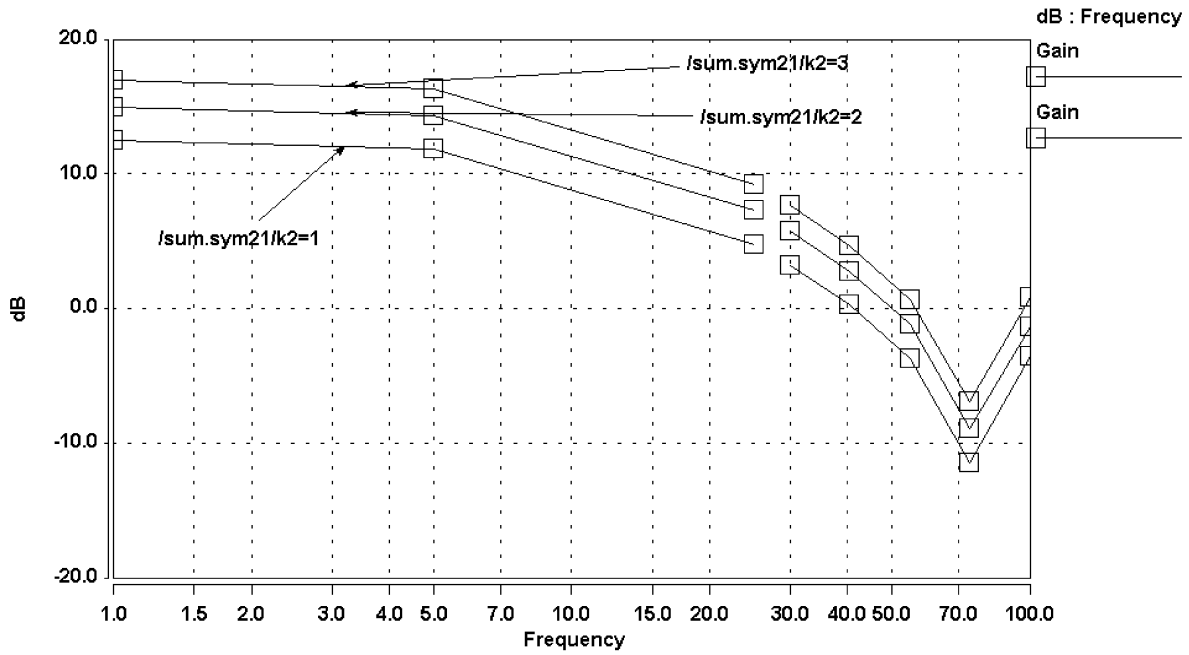

Fig. 6. Loop gain of the SVS algorithm for varying $K_{\rm vp}$, with $K_v = 1$, for RLC loads.

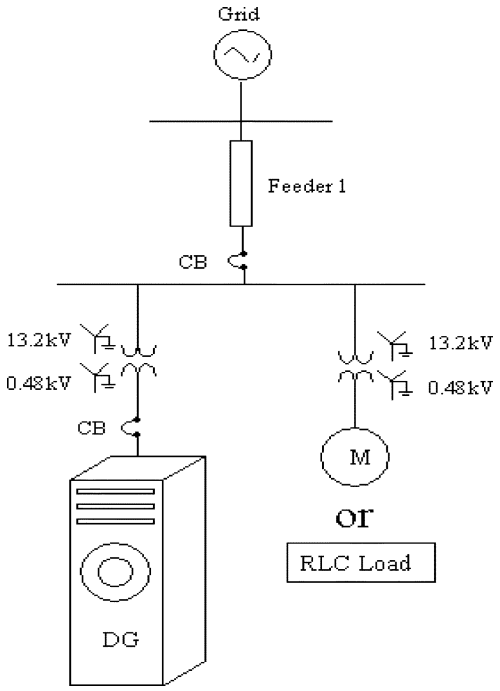

Fig. 7. Single line diagram for testing the anti-islanding scenario.

gains obtained by breaking the θ_v signal flow path in Fig. 1. All gains referred to in the analysis are calculated in per unit on the DG base. It can be seen the response is nearly flat for low frequencies (10 Hz and below) and droops down at higher frequencies. Gains greater than 0 dB are inherently unstable because it results in positive feedback under closed loop conditions with phase angle approximately zero (not shown in the plot). It can be observed that the load power levels did not affect the loop gain of the SFS algorithm. This implies that the power level of DG operation does not affect the SFS.

Similarly, Fig. 6 shows the open loop gain frequency response of SVS algorithm. As there are two gains to be set for the SVS, each gain ($K_{\rm vp}$ and K_v) is independently studied. In this case the loop gains are obtained by opening the $|V|$ signal flow path shown in Fig. 1. The loop gain characteristics of the SVS algorithm is flat at low frequencies (below 5 Hz). The magnitude of the gain is higher than 0 dB indicating that the SVS algorithm will be effective (i.e., unstable) for the gains shown in Fig. 6.

Compared with SFS loop gains, SVS loop gains are sensitive to the power level. Higher power level will reduce the gain. Therefore, the SVS gain has an additional coefficient Kvp to incorporate the power level variations.

The above frequency-domain study provided design space and guidelines for the SFS and SVS gain settings. The Section II-D discusses other design parameters, such as washout frequencies and time constants.

D. Washout and Power Regulation Time Constants

The schemes use a number of parameters ($\omega_{\rm f1}, \omega_{\rm f2}, K_{\rm vp}$, K_v, K_f) that have to be set appropriately for the algorithm to operate properly. The corner frequency $\omega_{\rm f1}$ is set to differentiate between a change in measured frequency or voltage due to variation in DGs operating point and other slow dynamics of the power system. Hence, $\omega_{\rm f1}$ is set to 0.1 Hz. Hence, voltage or frequency changes that occur in a time of less that 10 s can excite the anti-islanding algorithm. If the voltage or frequency change sustains for longer than 10 s then it is considered a change in the nominal operating condition. The corner frequency $\omega_{\rm f2}$ is set to 0.01 Hz. This is used to filter the measured voltage amplitude, which is then used to obtain the current command from the power command, as shown in Fig. 4. In case the DG terminal voltage rises, the anti-islanding algorithm tries to increase the power command, while the power regulation loop through $\omega_{\rm f2}$ lowers the reference current

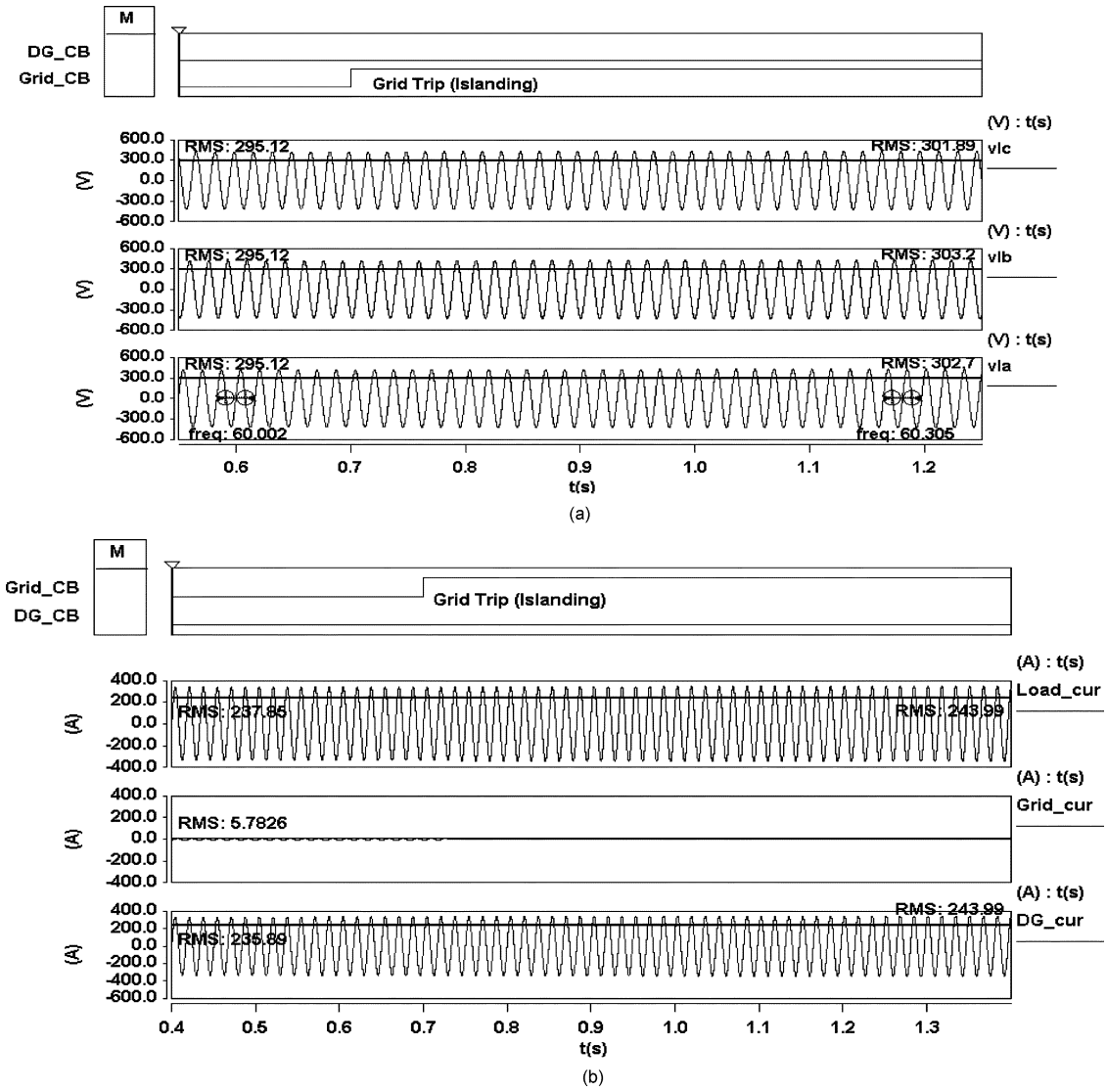

Fig. 8. Waveforms for the RLC load without anti-islanding protection: (a) load phase voltage and (b) current.

magnitude to maintain constant real and reactive power level. The corner frequency of ω_{f2} has been set to be decade lower than ω_{f1} in the anti-islanding algorithm, so that the change in current magnitude due to voltage regulation and anti-islanding do not counteract each other. The setting of 0.01-Hz corner frequency will also allow the DG prime mover to respond and change its power level in a time frame (of the order of 10 s) to a change in the measured output voltage [14].

The range of values for the SFS and SVS gain determined from the above analysis provides design space for time domain simulations of the DG system. The time domain simulations are application dependent and need to be considered on an individual basis. The time domain simulations will provide acceptance trade-off for the time to detect island.

III. Time–Domain Validation

In this work, Saber is used for both time–domain and frequency-domain simulations. The system in Fig. 7 is modeled in Saber with detailed inverter model, RLC load, and grid, which is modeled as a voltage source behind impedance.

The RLC resonant load as shown in Fig. 7 was first tested without any anti-islanding protection. The waveforms for this case are shown in Fig. 8. It can be observed from the voltage and current waveforms, that the DG continues to feed the RLC load and forms an island. The frequency and voltage drift by a small amount due to a minor difference in RLC values and due to the small numerical mismatch between the real and reactive power in the load and generator. However, the drifts in frequency and voltage magnitude are not sufficient to detect an islanding situation in an acceptable time frame (based on the passive anti-islanding limits on voltage and frequency set according to IEEE 1547).

Fig. 9 depicts the voltage and current at the DG terminals for the RLC load, for the case where the active anti-islanding algorithm is enabled. The gain settings used we the minimum gains that provides acceptable anti-islanding performance based the frequency domain analysis. Large SVS and SFS gains create waveform distortion and power quality degradation. The system was islanded at time 0.700 37 s by disconnecting the grid. The DG detected the island and tripped due to a drift in the frequency because of the active anti-islanding algorithm.

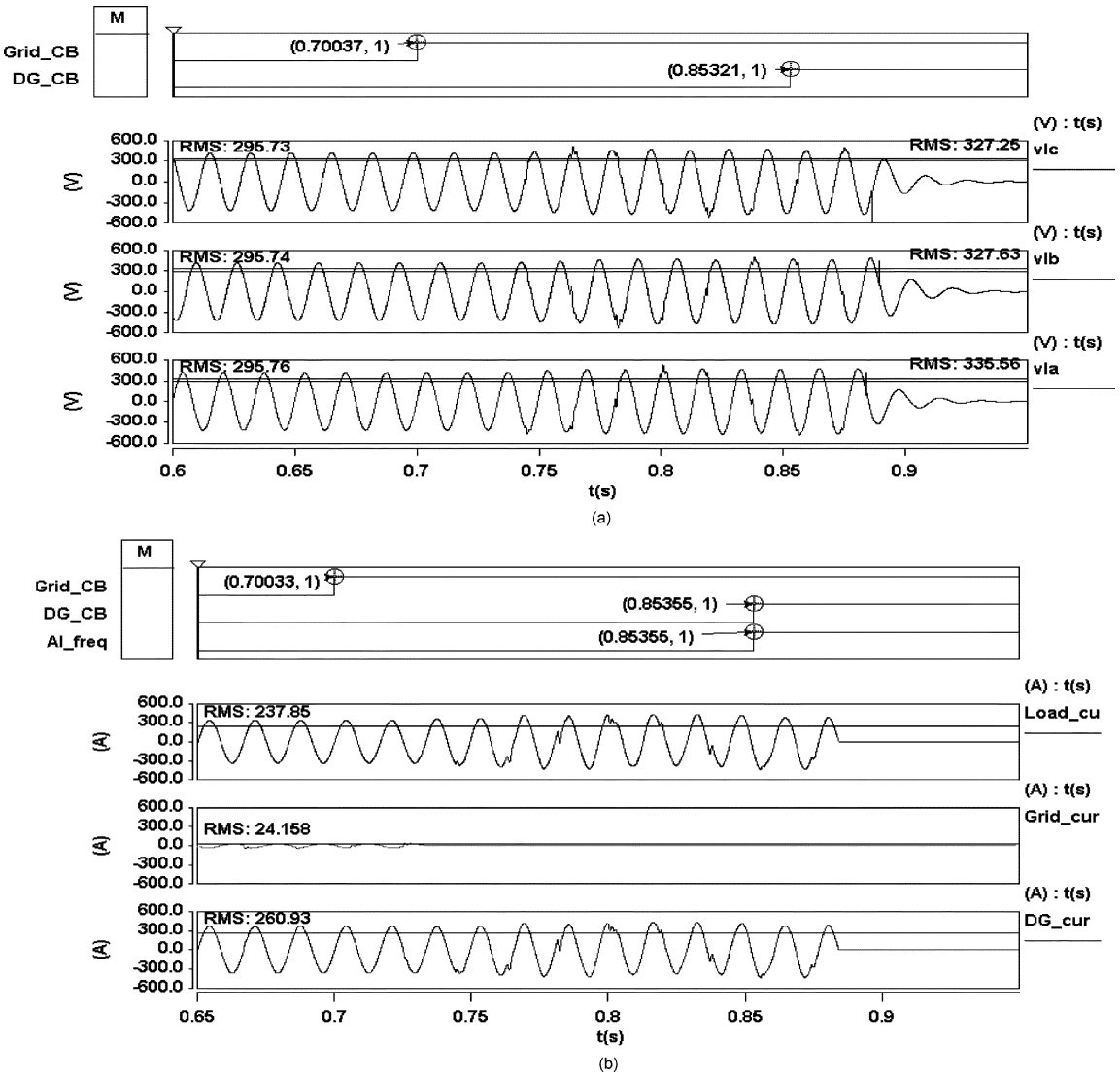

Fig. 9. Waveforms for RLC load with $K_f = 10$ and K_v and $K_{vp} = 2$: (a) load phase voltage and (b) current.

IV. Conclusion

This paper modeled and analyzed SFS and SVS anti-islanding schemes in frequency domain. The implications of the gains with respect to effectiveness and power variation were discussed. Time domain simulation was provided to validate the gain settings.

In frequency domain it has been observed that the SFS loop gain did not vary with the load power, while SVS loop gain varies with power level. The algorithm when tuned for rated DG power level will be effective under all realistic operating conditions.

The model presented in the paper will help the algorithms optimization. Sandia's schemes use a positive-feedback concept. The design for the positive feedback has usually been heuristic to date. The paper provided a rigorous approach to guide the design to ensure islanding can be detected, while the power quality degradation (due to overly large gain) is minimized.

The analysis approach can be extended to other anti-islanding schemes. Future work can be preformed to study these algorithms with dynamic load, such as motors.

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Vinod John (S'92–M'99) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Madras, in 1992, the M.S.E.E. degree from the University of Minnesota, Minneapolis, in 1994, and the Ph.D. degree from the University of Wisconsin, Madison, in 1999.

He was with General Electric Corporate Research and Development Center, Niskayuna, NY, from 1999 to 2002. Since June 2002, he has been with Northern Power Systems, Waitsfield, VT. His primary areas of interest are power converters and utility interface, microgrid power systems, and sustainable energy technologies.

Zhihong Ye (S'98–M'00) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1992 and 1994, respectively, and the Ph.D. degree from the Virginia Polytechnic Institute and State University (Virginia Tech), Blacksburg, in 2000.

Since September 2000, he has been with General Electric Company Global Research Center, Niskayuna, NY, where he is involved with several distributed generation programs, including power conditioning systems design for fuel cells, photovoltaics and microturbines, analysis and design of distributed generation and utility system interconnection, etc. His research interests are multiphase power conversion, power-conditioning systems for alternative and renewable energy, and power systems analysis with distributed generations. He has authored over 20 technical papers.

Dr. Ye is a member of Sigma Xi and the IEEE Power Electronics, Industry Applications, Industrial Electronics, and Power Engineering Societies.

Amol Kolwalkar (M'03) received the B.S. degree in electrical engineering from Sardar Patel College of Engineering (SPCE), Mumbai, India, in 1997 and the M.Tech. degree from the Indian Institute of Technology (IIT), Mumbai, in 2001.

Prior to joining IIT, he was with Tata Consulting Engineers, Mumbai. Currently, he is working with General Electric, Global Research Centre, Bangalore, India. His areas of interest include analysis of distributed generation systems and power electronics application in power systems.