1-V Low-Power Programmable Rail-to-Rail Operational Amplifier With Improved Transconductance Feedback Technique

Shanshan Dai, Xiaofei Cao, Ting Yi, Allyn E. Hubbard, and Zhiliang Hong

***Abstract*— A low-power process-independent programmable transconductance rail-to-rail operational amplifier (OpAmp) is proposed. It employs an improved transconductance feedback loop that senses the transconductance (g_{mT}) accurately and enforces it to be equal to the conductance of a reference resistor. Experimental results in a 0.13-μm standard CMOS technology under a 1–V power supply demonstrate a continuous programmable g_{mT} range from 87 to 165 μA/V with minimum fluctuation of ±2.4% and programmable deviation less than 4.5% from the reference value. The OpAmp achieves a unity-gain bandwidth of 3.7 MHz with a 95-pF load while only consuming 187 μA of quiescent current. The figure of merit of the proposed OpAmp is 1879 MHz·pF/mA.**

***Index Terms*— Constant transconductance, low power, operational amplifier, programmable, rail-to-rail.**

I. Introduction

As MODERN CMOS technology downscales, the reduction of supply voltage in CMOS integrated circuits has led to smaller common-mode input range for traditional operational amplifiers (OpAmp) with a single input differential pair and a reduced signal-to-noise ratio. The rail-to-rail amplifiers, with parallel-connected complementary p-channel and n-channel differential pairs in the input stage, are used to solve this problem by extending the common-mode input range from the negative supply rail to the positive supply rail. However, there are two limitations to the design and application of the rail-to-rail amplifiers. The first is that when the common-mode input voltage is in the middle of the positive and negative supply rails, the transconductance (g_{mT}) is double that when only one pair is operating near the positive (negative) rail. The large fluctuation of g_{mT} impedes power-efficient frequency compensation and introduces signal distortion [1]–[7]. The other limitation is that, like most other analog elements, the rail-to-rail OpAmp has a long design period, which slows down the design phase when integrated with digital circuits on one chip. Therefore, a programmable rail-to-rail OpAmp with constant small-signal behavior for VLSI cell libraries is highly time-efficient in modern mixed-signal chip design [6], [8], [9].

Many schemes have been proposed to equalize g_{mT}, such as constant square root summation [1], [2] for strong inversion region, constant current summation [3]– [7] for weak inversion region, transconductance compensation [10], feed-forward [9], bulk-driven [11], and transconductance feedback techniques [12]– [14]. The transconductance feedback technique has become especially popular among constant g_{mT} designs for its advantages of better constant g_{mT} behavior and programmable capability. The quasi-floating gate rail-to-rail amplifier [8] can achieve small g_{mT} fluctuation while being programmable, but the large area of the input coupling capacitors hampers its on-chip integration.

By sensing the input transconductance and representing it as two transconductor stages, the traditional transconductance feedback technique equalizes the transconductance sum of the two transconductor stages to that of a reference stage in the feedback module [12]–[14]. Continuous programmability can be achieved by tuning the tail current in the reference transconductor stage. However, one drawback is that small g_{mT} fluctuation can be achieved only at the expense of high power consumption. Moreover, the programmable g_{mT} value is highly process-dependent. Based on the traditional transconductance feedback technique, this paper represents the input transconductance as small-signal resistance in diode-connected form and uses a reference resistor as the reference value. The proposed technique shows a significant improvement in power consumption while achieving a similar constant g_{mT} performance and process-independent programmability with respect to the state of the art.

II. Rail-to-Rail Amplifier Architecture

Fig. 1 illustrates the block diagram of the proposed rail-to-rail amplifier. MN01–MN02 and MP01–MP02 form N–P complementary differential pairs used to provide rail-to-rail common-mode input range. The transconductance of the input stage g_{mT} is equal to ($g_{m,MN01} + g_{m,MP01}$). In the feedback module, blocks T_1 and T_2 are both transconductance amplifiers, the transconductance values of which are enforced

Manuscript received April 9, 2012; revised July 16, 2012; accepted August 31, 2012. Date of publication November 16, 2012; date of current version September 9, 2013. This work was supported in part by the National Natural Science Foundation of China under Grant 60876021 and the State Key Laboratory Project under Grant MS20080203.

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Digital Object Identifier 10.1109/TVLSI.2012.2220387

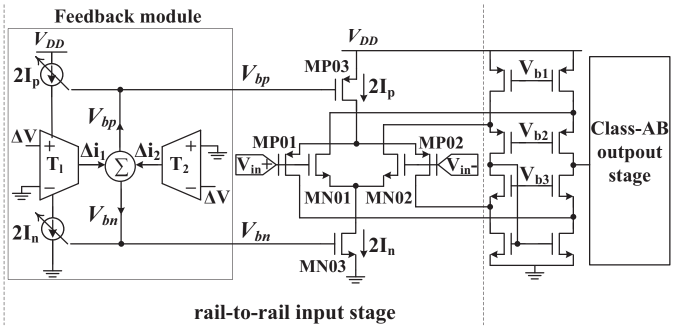


Fig. 1. Proposed rail-to-rail amplifier.

to be equal by the negative feedback. The feedback module also generates two tuning voltages V_{bn} and V_{bp} to adjust the tail currents in the input stage, to keep g_{mT} constant over the rail-to-rail common-mode input range.

III. g_{mT}-R Converter and Resistive Comparator in the Feedback Module

Fig. 2(a) shows a diode-connected nMOS transistor with its gate and drain connected together; its equivalent small-signal resistance $r_{eq,n}$ viewed from the drain side is given by

$$r_{eq,n} = \frac{1}{g_{mn} + g_{mb,n} + g_{ds,n}} \tag{1}$$

where g_{mn}, $g_{mb,n}$ and $g_{ds,n}$ correspond to nMOS transconductance, bulk transconductance, and drain-to-source conductance, respectively. By replicating input nMOS and pMOS transistor pairs in Fig. 1 with the same tail currents and making them diode-connected as in Fig. 2(b), the equivalent small-signal resistance $r_{eq,AB}$ across nodes A and B is

$$\begin{aligned} r_{eq,AB} &= \frac{2}{g_{mn} + g_{ds,n} + g_{mp} + g_{ds,p}} \\ &= \frac{2}{g_{mT} + g_{ds,n} + g_{ds,p}} \end{aligned} \tag{2}$$

where g_{mT} is the input transconductance of rail-to-rail amplifier. The bulk transconductance is not taken into account because the source nodes of nMOS and pMOS transistors are small-signal ground. Therefore, g_{mT} can be expressed as a function of the resistance $r_{eq,AB}$. Equation (2) indicates a way to realize a g_{mT}–R converter; constant transconductance can be achieved if $r_{eq,AB}$ is equalized over the entire common-mode range.

The feedback module in Fig. 1 is shown in Fig. 2(c). Suppose that

$$\begin{aligned} g_{mp26} &= g_{mp27} = g_{mf1} \\ g_{mp28} &= g_{mp29} = g_{mf2}. \end{aligned}$$

Since MP26–MP29 are identical transistors with same bias current, they have the same transconductance g_{mf}

$$g_{mf1} = g_{mf2} = g_{mf}. \tag{3}$$

The block T_1 in the feedback module is the g_{mT}–R converter. Replicas of the input transistor pairs MN19–MN20 and MP19–MP20 in diode-connected form are used as source degeneration resistors [15] for MP26–MP27. The tail currents of MN19–MN20 and MP19–MP20 mirror the tail currents $2I_n$ and $2I_p$ in the input stages by a ratio of 1:1, respectively. Two identical reference resistors R_1 and R_2 ($R_1 = R_2 = R_{ref}$) act as source degeneration resistors for MP28–MP29 in T_2. T_1 and T_2 are unbalanced by a dc input voltage ΔV with the polarities shown in Fig. 2(c). Assuming the transconductance of T_1 is g_{m1} and the transconductance of T_2 is g_{m2}, the output currents Δi_1 from T_1 and Δi_2 from T_2 can be expressed as functions of source degeneration resistance $r_{eq,AB}$ and $r_{eq,CD}$, respectively, as

$$\begin{aligned} \Delta i_1 &= g_{m1} \cdot \Delta V = \frac{g_{mf1}}{1 + g_{mf1}\left(\frac{r_{eq,AB}}{2}\right)} \cdot \Delta V \\ &= \frac{g_{mf1}}{1 + g_{mf1}(g_{mT} + g_{ds,n} + g_{ds,p})^{-1}} \cdot \Delta V \end{aligned} \tag{4}$$

$$\begin{aligned} \Delta i_2 &= g_{m2} \cdot (-\Delta V) = -\frac{g_{mf2}}{1 + g_{mf2}\left(\frac{r_{eq,CD}}{2}\right)} \cdot \Delta V \\ &= -\frac{g_{mf2}}{1 + g_{mf2} \cdot R_{ref}} \cdot \Delta V \cdot \end{aligned} \tag{5}$$

A current summation stage between T_1 and T_2 converts the sum of currents Δi_1 and Δi_2 into two tuning voltages V_{bn} and V_{bp} to control the tail current sources in both the feedback module and the input stage. For the case $\Delta i_1 + \Delta i_2 > 0$, in other words, $(g_{mT} + g_{ds,n} + g_{ds,p})^{-1} < R_{ref}$, the tuning voltages will turn off the tail current source transistors a bit in order to decrease g_{mT} until $(g_{mT} + g_{ds,n} + g_{ds,p})^{-1} = R_{ref}$

$$g_{mT} = R_{ref}^{-1} - g_{ds,n} - g_{ds,p}. \tag{6}$$

In this way, the current summation stage serves as a resistive comparator for $(g_{mT} + g_{ds,n} + g_{ds,p})^{-1}$ and R_{ref}. Since $g_{ds,n}$ and $g_{ds,p}$ are small enough to be ignored in comparison

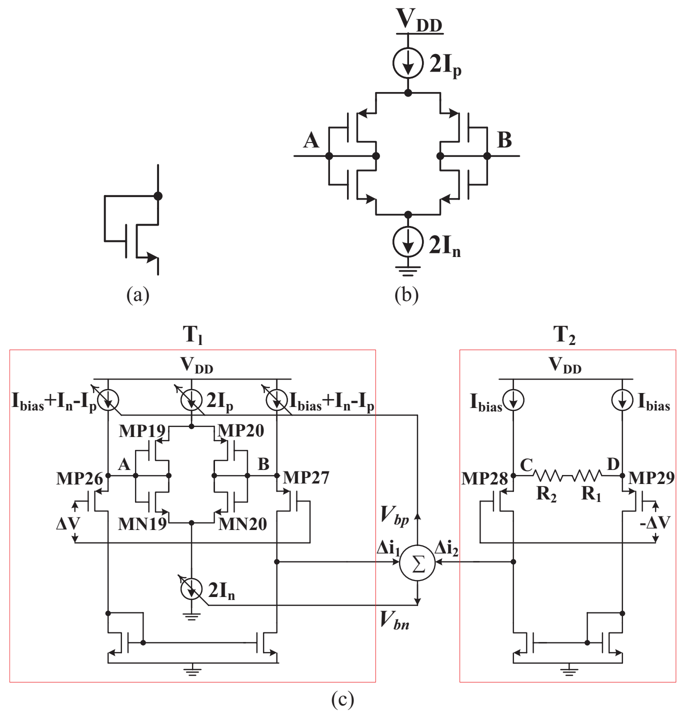
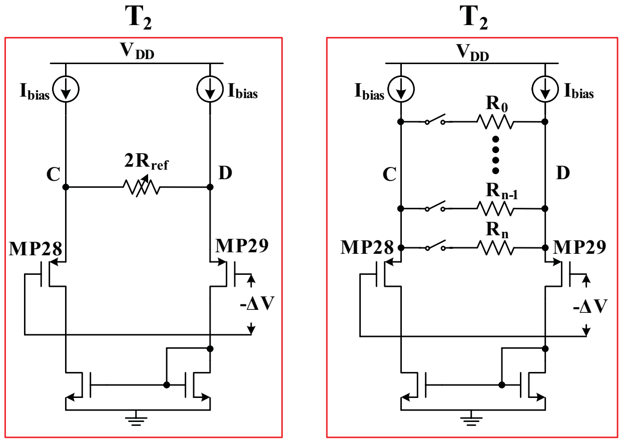


Fig. 2. (a) Diode-connected nMOS. (b) g_{mT}–R converter. (c) g_{mT}–R converter and resistive comparator in the feedback module.



(a) (b)

Fig. 3. (a) Continuous programmable realization using off-chip resistor in T_2. (b) Discrete programmable realization using on-chip resistor array in T_2.

with g_{mT}, the dynamic feedback loop can equalize g_{mT} to the reciprocal of reference resistance R_{ref} ($g_{mT} \cong R_{ref}^{-1}$) over the entire common-mode input range.

According to (6), g_{mT} programmability can be achieved by adjusting the reference resistance R_{ref} in T_2 due to the dynamic feedback. If R_{ref} is realized by an off-chip tunable resistor as shown in Fig. 3(a), continuous programmability can be achieved. Fig. 3(b) shows the discrete programmable realization when the on-chip reference resistor array is controlled by logic signals. And the programmable g_{mT} value only depends on the value of R_{ref} regardless of input transistor dimensions, input matching condition, and process parameters.

IV. Feedback Module of Rail-to-Rail OpAmp

The overall circuit implementation of the feedback module is shown in Fig. 4. In addition to T_1 (g_{mT}–R converter), T_2, and the current summation stage (resistive comparator) mentioned in Section III, the feedback module also includes a dynamic bias current generator to provide a current of ($I_{bias} + I_n - I_p$) for the two current sources MS1 and MS2 in T_1. The folded-cascode transimpedance amplifier structure is employed in the current summation stage to convert the output current summation of T_1 and T_2 to two controlling voltages V_{bn} and V_{bp}. The input transistor pairs and their tail current sources in Fig. 1 are replicated by six transistors MN09–MN11 and MP09–MP11 with the same transistor sizes and currents. The drain terminals of MN09 (MP09) and MN10 (MP10) are connected together to cancel out the input differential signals. Thus, the tail current $2I_n$ ($2I_p$) of input stage can be sensed and measured by MP12 (MN12). The current $2I_n$ ($2I_p$) is copied to MN18 (MP18) in T_1 by two current mirrors MP12, MP13 (MN12, MN13) and MN14, MN18 (MP14, MP18) with ratios of 4:1 and 1:4, respectively, to ensure that the transconductance of MN19 and MN20 (MP19 and MP20) equals that of MN01 and MN02 (MP01 and MP02) in Fig. 1. The current flowing through MP16 is set to be $I_{bias}/2$, which is one-half of the currents through current sources MS3–MS4 in T_2 and MP21–MP22 in the current summation stage. MP15–MP16 and MN15–MN16 realize the current summing and subtracting, thus the current through MP17, I_{MP17}, is equal to $(I_{bias}+I_n-I_p)/2$. Hence, the dynamic current sources MS1 and MS2 in the g_{mT}–R converter (T_1) can obtain the currents of ($I_{bias} + I_n - I_p$) by simply mirroring I_{MP17} by a factor of 2. In sum, the dynamic bias current generator is used to generate four current sources for T_1: MS1 and MS2 with same current of ($I_{bias} + I_n - I_p$), MN18 with current of $2I_n$, and MP18 with current of $2I_p$, so that the following two objectives can be achieved: 1) replicating the input n- (p-) transconductance g_{mn} (g_{mp}) to that of MN19–MN20 (MP19–MP20); and 2) ensuring that the currents and transconductance of MP26–MP29 are the same.

A. Stability Analysis of the Feedback Loop

Apparently, the proposed feedback loop is a common-mode feedback loop because the differential input signals are cancelled in the feedback module. It must be stable to guarantee the stability of the main OpAmp. In Fig. 4, the only high impedance node P forms the dominant pole p_0 of the feedback module. The first nondominant pole p_1 is located at nodes A and B (two nodes contribute one single pole only). The other nondominant poles include p_{nd} (p_{pd}) located at drain terminals of MN09–MN10 (MP09–MP10), and p_{ns} (p_{ps}) at source terminals of MN19–MN20 (MP19–MP20), etc. These poles can be expressed as follows:

$$p_0 = \frac{1}{r_o.(C_{bp} + C_C)} \tag{7}$$

$$p_1 = \frac{g_{mn} + g_{mp} + g_{mf1}}{C_A} \tag{8}$$

$$p_{nd} = \frac{g_{mp12}}{C_{nd}}, \quad p_{pd} = \frac{g_{mn12}}{C_{pd}} \tag{9}$$

$$p_{ns} = \frac{2g_{mn}}{C_{ns}}, \quad p_{ps} = \frac{2g_{mp}}{C_{ps}} \tag{10}$$

where r_o is the output resistance of node P. C_{pb}, C_A, C_{nd} (C_{pd}), and C_{ns} (C_{ps}) are the parasitic capacitance of nodes P, A, the drain terminals of MN09–MN10 (MP09–MP10) and the source terminals of MN19–MN20 (MP19–MP20), respectively. g_{mp12} and g_{mn12} are the transconductance of MP12 and MN12, respectively. To avoid instability, a capacitor C_C is added between node P and ground to move the dominant pole toward the frequency origin. By breaking the connection between node P and the gate of MP25, and applying a small-signal voltage v_{in} at the gate of MP25, the simplified feedback loop transfer function is calculated as

$$\begin{aligned} LG(s) &= \frac{r_o}{\left(1+\frac{s}{p_0}\right)\left(1+\frac{s}{p_1}\right)} \cdot \frac{di_{out}}{dv_{in}} \\ &= \frac{r_o}{\left(1+\frac{s}{p_0}\right)\left(1+\frac{s}{p_1}\right)} \cdot \frac{d(\Delta V.g_{m1})}{dv_{in}} \\ &= \Delta V.\frac{r_o}{\left(1+\frac{s}{p_0}\right)\left(1+\frac{s}{p_1}\right)} \cdot \left(\frac{\partial g_{m1}}{\partial g_{mn}} \cdot \frac{\partial g_{mn}}{\partial v_{gsn}} \cdot \frac{\partial v_{gsn}}{\partial i_n}\right. \\ &\qquad \left. \cdot \frac{\partial i_n}{\partial v_{in}} + \frac{\partial g_{m1}}{\partial g_{mp}} \cdot \frac{\partial g_{mp}}{\partial v_{gsp}} \cdot \frac{\partial v_{gsp}}{\partial i_p} \cdot \frac{\partial i_p}{\partial v_{in}}\right) \end{aligned}$$

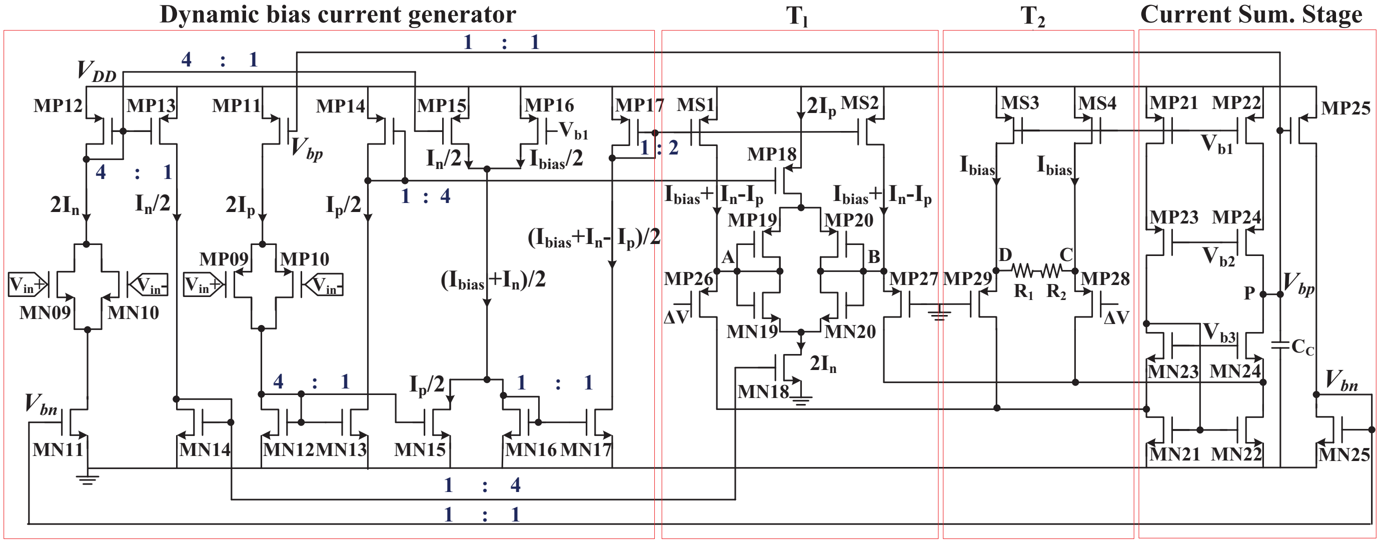


Fig. 4. Circuit schematic of the feedback module.

$$= \Delta V. \frac{r_o}{\left(1+\frac{s}{p_0}\right)\left(1+\frac{s}{p_1}\right)} \cdot \frac{g_{mf1}^2}{\left(g_{mf1}+g_{mn}+g_{mp}\right)^2} \cdot \left(\frac{1}{\left(1+\frac{s}{p_{nd}}\right)\left(1+\frac{s}{p_{ns}}\right)} \cdot \frac{g_{mp25}}{g_{mn}} \cdot \frac{\partial g_{mn}}{\partial v_{gsn}} + \frac{g_{mp11}}{g_{mp}} \cdot \frac{\partial g_{mp}}{\partial v_{gsp}} \cdot \frac{1}{\left(1+\frac{s}{p_{pd}}\right)\left(1+\frac{s}{p_{ps}}\right)} \right) \quad (11)$$

where the values of $\partial g_{mn}/\partial v_{gsn}$ and $\partial g_{mp}/\partial v_{gsp}$ depend on the operation region of the input transistors, g_{mp25} and g_{mp11} are the transconductance of MP25 and MP11, respectively. Under the worst condition of $\Delta V = 100$ mV, the simulated Bode plot of the feedback loop for the nominal common-mode input dc voltage, loop gain, phase margin and unity-gain bandwidth (UGB) versus the common-mode input voltage are shown in Fig. 5. Similar to the small-signal behavior of traditional transconductance feedback module, the feedback loop gain (11) reaches its maximum in the middle of common-mode input voltage, leading to the worst case of phase margin. Since the UGB of the common-mode feedback module should be no less than that of the main OpAmp, it is the feedback module that limits the speed of the proposed rail-to-rail amplifier.

B. Mismatch and Power Constraints on Programmability

Equation (6) holds exactly only when MP26–MP29 have the same transconductance, that is, $g_{mf1} = g_{mf2} = g_{mf}$, as shown in (3). The relative mismatches in the feedback module will inevitably result in $g_{mf1} \neq g_{mf2}$. To explore this impact, the precise expression of g_{mT} without any approximation is

$$g_{mT} = \left(\frac{1}{g_{mf2}} - \frac{1}{g_{mf1}} + R_{ref} \right)^{-1} - g_{ds,n} - g_{ds,p}. \quad (12)$$

Suppose that $g_{mf1} = g_{mf} + \Delta g_{mf}$, $g_{mf2} = g_{mf}$, and that $g_{ds,n}$ and $g_{ds,p}$ are small enough to be ignored, and so are their variations $\Delta g_{ds,n}$ and $\Delta g_{ds,p}$. Now, the partial derivative of g_{mT} with respect to g_{mf1} and g_{mf2} can be derived as

$$\frac{\partial g_{mT}}{g_{mT}} = \frac{1}{g_{mT}} \left[g_{mT}|g_{mf1} = g_{mf} + \triangle g_{mf}, g_{mf2} = g_{mf} - g_{mT}|g_{mf1} = g_{mf2} = g_{mf} \right] \cong -\frac{1}{g_{mT} \cdot g_{mf} R_{ref}^2} \cdot \frac{\Delta g_{mf}}{g_{mf}} \cong -\frac{1}{g_{mf} \cdot R_{ref}} \cdot \frac{\Delta g_{mf}}{g_{mf}}. \quad (13)$$

In particular, it can be noticed that Δg_{mf} accounts for not only current mirror inaccuracies in dynamic bias current generator but also for device mismatches among MP26–MP29. The former varies as the common-mode input voltage changes, and thus results in both g_{mT} fluctuation and deviation from R_{ref}^{-1}. The latter, however, only brings programmable inaccuracy.

In (13), $(g_{mf} \cdot R_{ref})$ in the denominator is expected to be large in order to decrease g_{mT} sensitivity to mismatch between g_{mf1} and g_{mf2}. At least, $(g_{mf} \cdot R_{ref})$ should be larger than unity, and this in turn means that the reference resistance R_{ref} has a minimum value of

$$R_{ref,min} = \frac{1}{g_{mf}}. \quad (14)$$

According to (6) and (14), one upper bound of g_{mT} is

$$g_{mT-\max} = g_{mf}. \quad (15)$$

Meanwhile, the currents through MS1 and MS2 make sense only with positive values, which means $(I_{bias} + I_n - I_p) > 0$. Therefore, in order to achieve constant and accurate g_{mT}, the maximum $g_{mT-\max}$ of the proposed OpAmp is derived as

$$g_{mT-\max} = R_{ref\,min^{-1}} = \min[g_{mf}, g_{mp}(I_{bias})] \quad (16)$$

where $g_{mp}(I_{bias})$ is equal to the transconductance of input pMOS transistor biased with current I_{bias}.

On the other hand, however, sufficient feedback-loop gain needs to be maintained to provide accurate tuning voltages for

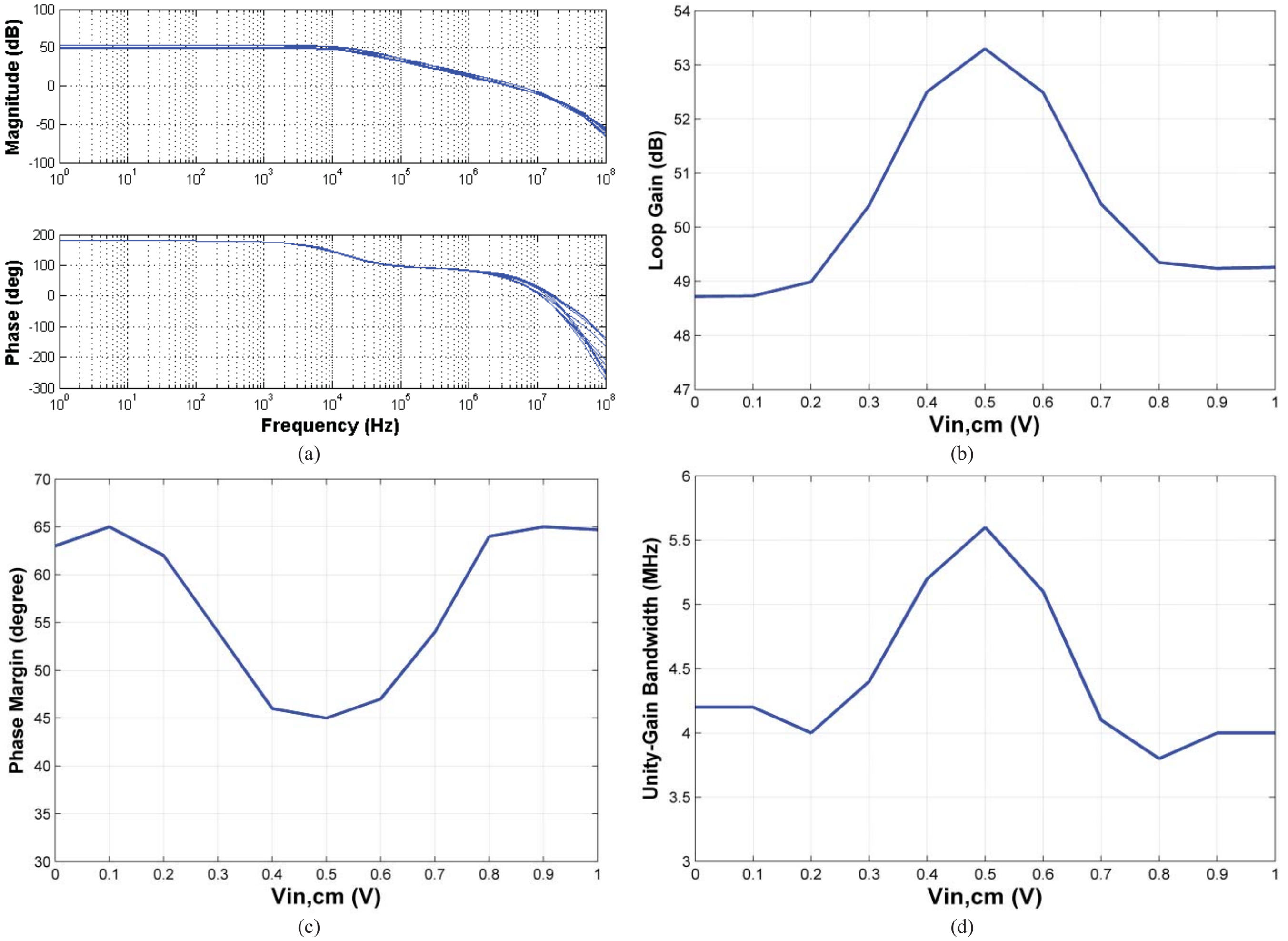


Fig. 5. (a) Bode plot of the feedback loop. (b) Loop gain of the feedback module versus $V_{in,cm}$. (c) Phase margin of the feedback module versus $V_{in,cm}$. (d) UGB of the feedback module versus $V_{in,cm}$ (simulation results under the worst condition of $\Delta V = 100$ mV).

a constant g_{mT}. Thus, R_{ref} should not be too large; otherwise, it will decrease the feedback-loop gain significantly as a source degeneration resistor. Because both g_{mf} and $g_{mp}(I_{bias})$ in (16) are monotonically increasing functions of the bias current I_{bias}, a wide programmable g_{mT} range can be obtained in expense of power consumption by increasing I_{bias}.

In addition to mismatch between g_{mf1} and g_{mf2}, the invariance and accuracy of g_{mT} also depend on the relative mismatches between the replica pair MN19–MN20 (MP19–MP20) and the input differential pair MN01–MN02 (MP01–MP02). These mismatches include device mismatch and current mismatch. Device mismatch is dominated by threshold voltage difference ΔV_T and current factor ($\beta = \mu C_{ox} W/L$) difference $\Delta\beta$, both of which have a Gaussian distribution with zero mean and a sigma inversely proportional to the square root of device area

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{W \cdot L}} \tag{17}$$

$$\frac{\sigma(\Delta\beta)}{\beta} = \frac{A_\beta}{\sqrt{W \cdot L}} \tag{18}$$

where A_{VT} and A_β are technology-dependent constants, W is the width of gate, and L is the length. Current mismatch of $\sigma(\Delta I)$, taking the nMOS replica pair for example, is the current error brought by current mirrors of MN03, MN11, MP12, MP13 and MN14, MN18. Taking these mismatches into account, the relative gate-to-source voltage mismatch can be derived as

$$\sigma(\Delta V_{GS}) = \sqrt{\sigma^2(\Delta V_T) + \frac{1}{(g_m/I)^2}\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \frac{1}{(g_m/I)^2}\left(\frac{\sigma(\Delta I)}{I}\right)^2} \tag{19}$$

where g_m/I is the transconductance–current ratio (also called transconductance efficiency) of the relative transistor [16], [17].

The large feedback loop gain forces the sum of the output currents Δi_1 from T_1 and Δi_2 from T_2 to be zero. The two currents can be rewritten as

$$\Delta i_1 = \frac{V_{AB} - \sum \Delta V_{GS,n}}{2 \cdot g_{mn}^{-1}} + \frac{V_{AB} + \sum \Delta V_{GS,p}}{2 \cdot g_{mp}^{-1}} \tag{20}$$

$$\Delta i_2 = -\frac{V_{CD}}{2R_{ref}} \tag{21}$$

$$\Delta i_1 + \Delta i_2 = 0 \tag{22}$$

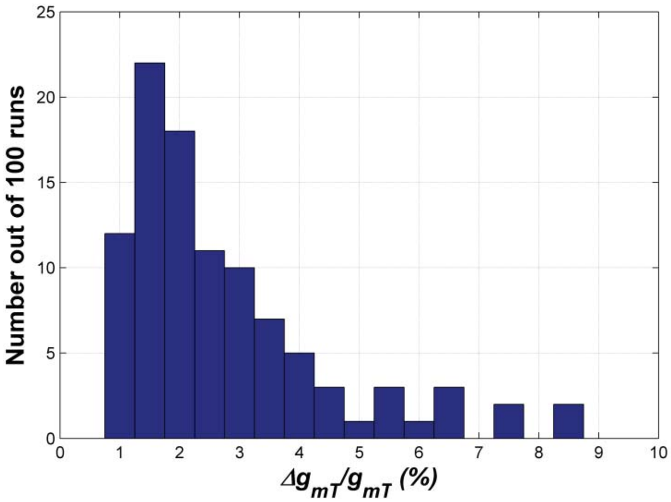


Fig. 6. One-hundred Monte Carlo process variation and mismatch simulation results.

where $\Sigma\Delta V_{GS,n(p)}$ accounts for the sum of the relative gate-to-source voltage differences between MN19–MN20 (MP19–MP20) and the input pair MN01–MN02 (MP01–MP02), thus $\Sigma\Delta V_{GS,n(p)} = \Sigma\Delta V_{GS,n(p),19} + \Sigma\Delta V_{GS,n(p),20}$. V_{AB} and V_{CD} are the voltages across nodes A and B, and nodes C and D, respectively. Their expressions are given by

$$V_{AB} = \frac{g_{mf1} \cdot g_{mT}^{-1}}{1 + g_{mf1} \cdot g_{mT}^{-1}} \cdot \Delta V \tag{23}$$

$$V_{CD} = \frac{g_{mf2} \cdot R_{ref}}{1 + g_{mf2} \cdot R_{ref}} \cdot \Delta V. \tag{24}$$

By combining (20)–(24), the expression of g_{mT} and its variation caused by $\Sigma\Delta V_{GS,n}$ and $\Sigma\Delta V_{GS,p}$ are derived as

$$g_{mT} = \frac{R_{ref}^{-1} V_{CD} + \left(g_{mn}.\sum \Delta V_{GS,n} - g_{mp}.\sum \Delta V_{GS,p}\right)}{V_{AB}} \tag{25}$$

$$\partial g_{mT} = \frac{(g_{mT} + g_{mf1})^2}{g_{mf1}^2} \cdot \left[\frac{\partial(g_{mn} \cdot \Sigma\Delta V_{GS,n})}{\Delta V} - \frac{\partial(g_{mp} \cdot \Sigma\Delta V_{GS,p})}{\Delta V}\right]. \tag{26}$$

For $V_{in,cm}$ values close to ground, both input nMOS pair and replica pair MN19–MN20 are turned off. As a result, ∂g_{mT} is not affected by $\Sigma\Delta V_{GS,n}$. Similarly, for $V_{in,cm}$ values close to V_{DD}, $\Sigma\Delta V_{GS,p}$ does not affect ∂g_{mT}, either. The variance and inaccuracy of g_{mT} caused by the mismatches between the replicas and input pairs can be decreased by applying a large ΔV to T1 and T2 according to (26) or/and by increasing the dimensions of the input pairs to decrease the influence from $\Sigma\Delta V_{GS,n(p)}$, according to (17)–(19). The effect of transistor mismatches was modeled by Monte Carlo analysis with 100 iterations, using the process parameter mismatches of the corresponding 0.13-μm CMOS process, as shown in Fig. 6. The statistic tells us the possibility that error greater than 1.5% will decrease exponentially.

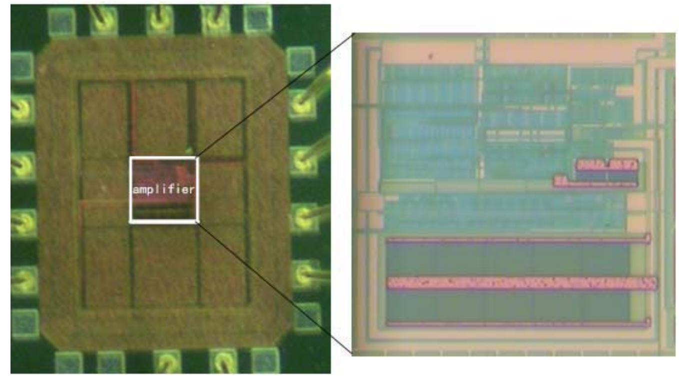


Fig. 7. Chip microphotograph.

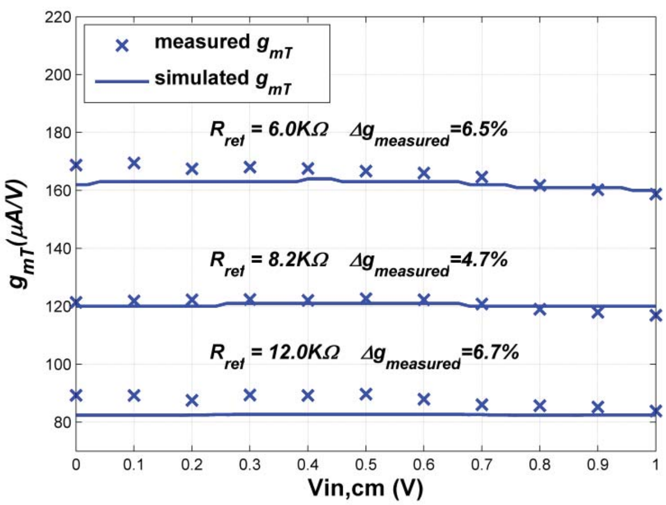


Fig. 8. Measured and simulated input transconductance g_{mT} versus $V_{in,cm}$.

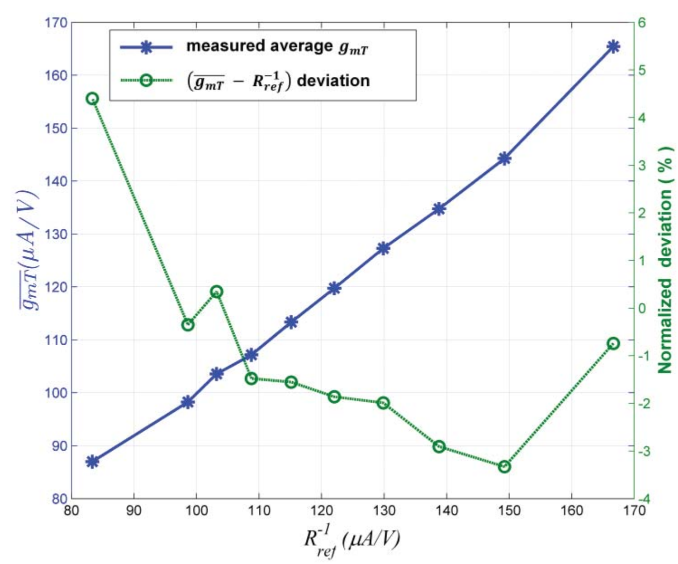


Fig. 9. Measured input stage transconductance $\overline{g_{mT}}$ versus R_{ref}^{-1}.

V. Simulation and Experimental Results

The proposed programmable rail-to-rail OpAmp was designed to operate with 1-V power supply, and fabricated in

TABLE I
PERFORMANCE COMPARISON

	[7]	[8]	[10]	[11]	[13]	This paper
Process	0.8-μm	0.8-μm	0.8-μm	0.35-μm	0.35-μm	0.13-μm
Supply voltage	1.0	3.0	3.0	1.0	1.5	1.0
Minimum $\Delta g_m / g_m$	±10%	±2.5%*	~ ±4.6%	±5%	±1.5%	±2.4%
Load	1 MΩ || 15 pF	5 pF	1MΩ || 15 pF	1MΩ || 17 pF	180 pF	20 KΩ || 95 pF
DC gain (dB)	74.7	102*	95.1	76.2	80	60
Current consumption (mA)	0.136	3.3	1.6	0.358	1.1	0.187
Unity-gain frequency (MHz)	1.8	100	17.5	8.1	1.1	3.7
FOM (MHz · pF/mA)	199	150	164	385	180	1879
Phase margin	57°	60°*	60°	63°	89°	72°
SR^+/SR^-	NA	150 (V/μs)*	16.26/16.28 (V/μs)	2.74/5.02 (V/μs)	2.52/2.43 (V/μs) (=130 pF)	1.74/1.59 (V/μs)
Die area (mm^2)	0.18 mm^2	0.1 mm^2	0.081 mm^2	0.0532 mm^2	0.09 mm^2	0.0289 mm^2

*Simulation results.

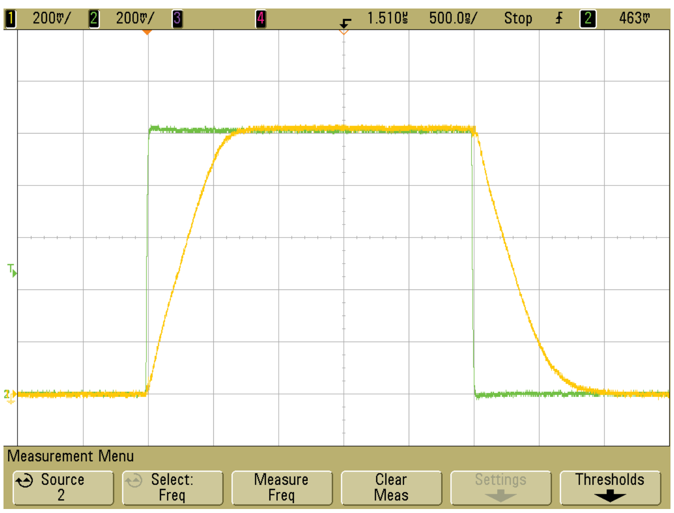


Fig. 10. Experimental time-domain pulse response for 1-V_{PP} 200-kHz input signals in noninverting unity-gain configuration with a capacitive load of 95 pF. Horizontal scale 500 ns/div. Vertical scale 0.2 V/div.

a standard 0.13-μm CMOS process with threshold voltages of pMOS and nMOS transistors around –0.38 and 0.4 V, respectively. Fig. 7 shows a microphotograph of the fabricated chip. The core area is 0.17 × 0.17 mm.

The bias current I_{bias} in the feedback module is designed to be 13 μA for low-power implementation. For measurements, a dc input voltage ΔV of 70 mV is applied to the transconductance amplifiers (T_1 and T_2) in the feedback module. Fig. 8 illustrates the simulated and measured values of g_{mT} versus the common-mode input range in open-loop configuration. With minimum fluctuation ±2.4% and maximum fluctuation ±3.4%, g_{mT} can be tuned from 87 to 165 μA/V by adjusting the reference resistance R_{ref} from 12.0 to 6.0 KΩ. To validate the programmable accuracy, $\overline{g_{mT}}$ versus R_{ref}^{-1} characteristic and normalized deviation between $\overline{g_{mT}}$ and R_{ref}^{-1} in percentage are shown in Fig. 9, where $\overline{g_{mT}}$ is the average input transconductance over the entire common-mode voltage range for a given R_{ref}. Very small measured $\overline{g_{mT}}$ deviation (within 4.5%) from the reference value R_{ref}^{-1} confirms the accurate programmability of the proposed OpAmp, as expected.

Fig. 10 depicts the experimental large-signal transient response by application of a 1-V_{PP} 200-KHz input square wave in noninverting unity-gain configuration. The measured input dc offset voltage ranges from 5.4 to 3.2 mV when the common-mode input voltage changes from 0 to 1 V. The OpAmp including a class-AB output stage achieves a UGB of 3.7 MHz with a load capacitor 95 pF and a power consumption of 187 μW, when R_{ref} is equal to 8.2 KΩ. The performance comparison with reported rail-to-rail OpAmps is summarized in Table I, and the figure of merit (FOM) of 1879 MHz · pF/mA shows the high power efficiency of this method.

VI. CONCLUSION

This paper presented a precisely process-independent programmable rail-to-rail circuit technique suitable for VLSI cell libraries with good constant-g_{mT} behavior. The implementation of the proposed circuit is realized by an improved transconductance feedback technique that employs a novel g_{mT}–R converter and a resistive comparator to enforce g_{mT} to equal the reciprocal of a reference resistance R_{ref}. As a result, both the programmability and constant behavior of g_{mT} are robust and universal regardless of the operation region and matching condition of input transistor pairs. The measured results of 1-V input/output rail-to-rail OpAmp verified the power-efficiency, high programmable accuracy, and small g_{mT} fluctuation.

ACKNOWLEDGMENT

The authors would like to thank the anonymous reviewers for their help, which improved the quality of this paper. The authors would also like to thank J. M. Carillo for his valuable comments and suggestions.

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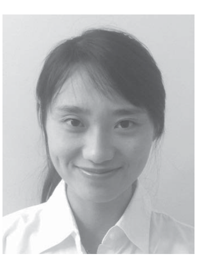

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