

CLDT: A COMBINATIONAL LOGIC DESIGN TOOL FOR USE IN ELECTRICAL AND COMPUTER ENGINEERING CURRICULA

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1. INTRODUCTION

Within the electrical and computer engineering curriculum, fundamental theories and concepts are taught that provide tools to be used by students in their upcoming careers. These topics are traditionally taught in a classroom by professors engaging in discussion with the student. However, a lack of resources exists outside of the classroom to aid the student in the understanding of these topics. A survey of available online tools resulted in the conclusion that no purely assessment tools exist (Morsi, 2004). This paper describes a ‘work in progress’ project that aims to complete the pilot tool “Interactive Karnaugh Map Evaluator” (available at www.ece-edu.com) and produce a complete interactive online assessment tool to assess students’ knowledge of the process of designing and implementing a combinational logic circuit.

The use of computer technology in engineering education has been an ongoing area of research for the past decade. Computers have become a very integrated component of our life and it only seems natural to make the most of them by using them in the educational process of engineering. Computers have become an essential computation tool for students in all engineering and engineering technology disciplines. Computer based learning has proven to be an accepted learning practice that can improve the educational process for students.

Teaching methods in an engineering classroom vary from the traditional black/white board style to the completely online style of teaching. LeMaster (2000) states that the use of electronic media and web tools in conjunction with classroom lectures (that is using the Power Point presentations in class as well as posting them on a web-site), although time consuming in the preparation process, are received well by students in his department and in general are well received.

Different forms of computer technology based education exist but there is no application that is considered as an online practice tool for students in Electrical and Computer Engineering. Assessment tools provide the ability to provide the user with the reassurance and validation of their knowledge as well as an opportunity to practice applying the knowledge acquired in the classroom.

A number of online tools exist in the area of digital design (Logic Works, LogiSym, KarnaughMap 1.2, Electronics Workbench, Java KV diagram and logic minimization, Embed karnaugh, Karnaugh Minimizer, and Karno). However, these tools are what the authors consider as ‘homework solvers’ where the students can in theory input a question assigned to them and in turn are given the answer by the software either in a tutorial like manner or as a correction to a wrong answer being input. This takes away the students’ chance of solving the problems themselves so they have little knowledge of whether they have applied the techniques learned in the classroom correctly.

The proposed work will entail developing a random truth table generator that ties into the Karnaugh Map evaluator tool the result of which would integrate into a digital circuit implementation tool. Each stage of the tool is interactive and ‘just-in-time’ assessed. In order to ensure a student completely understands the design process concept, the solution is not simply provided. The problem is solved in a step-by-step fashion. In doing this, the student can actually see the derivation of an answer rather than be provided with hints in order to achieve an answer.

2. COMBINATIONAL CIRCUIT DESIGN PROCESS

A digital system can be represented by a truth table (Figure 1) which is a table that correlates all possible input combinations of a system with the output.

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 1. Truth Table

A truth table can be mapped into a Karnaugh Map (Figure 2(a)) to ease the process of simplification. A Karnaugh map is a visual representation that allows the grouping of adjacent Boolean values on the map. Each cell in the K- Map represents a minterm (sum-of-product (SOP) expression) or maxterm (product-of-sum (POS) expression) of the switching function represented. Due to the layout of Karnaugh maps, grouping adjacent minterms/maxterms together can help cancel redundant variables and in turn minimize the overall expression. Groups made on a Karnaugh map are made in powers of two (1, 2, 4, 8, etc.).

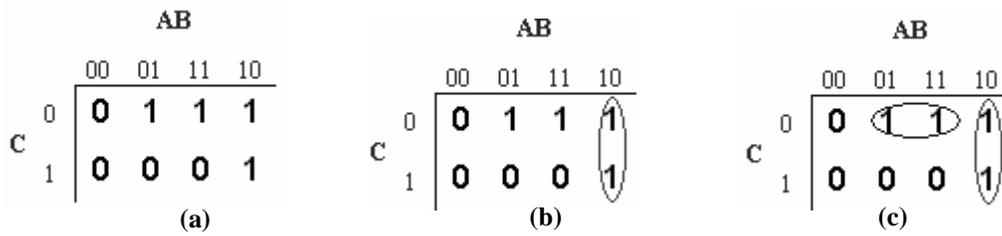


Figure 2. K-Map grouping

A Karnaugh map is solved by selecting the largest grouping of uncovered minterms (or maxterms). An expression is derived that equates to the covered cells. In Figure 2(b), the minterms in the right-most column are grouped resulting in the product term AB' (since all possible scenarios involving C are covered). This is repeated for the remaining uncovered minterms. The result is shown in Figure 2(c). The resulting expression is $AB' + BC'$.

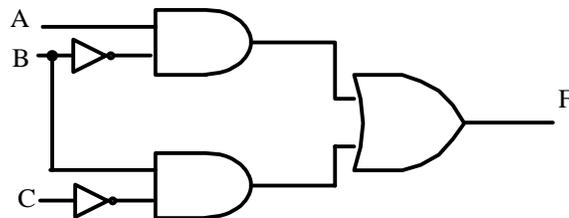


Figure 3. Circuit implementation in AND, OR, and NOT gates

Figure 3 shows the AND, OR, NOT circuit implementation of the Boolean Expression derived in Figure 2(c).

3. CLDT TOOL

The CLDT tool is intended as a tool that allows students to practice the complete process of designing combinational circuits. The tool allows practice in the three stages of the design process. The Truth Table phase, the KMap phase, and the circuit implementation phase. The CLDT is intended as an assessment tool that will provide students with randomly generated problem statements and checks for correctness of their answers. The tool will provide a 'correct' or 'incorrect' response. No solutions are provided since the intention of the tool is to be a practice tool not a homework helper.

This research is a "work in progress" NSF funded project (NSF EEC-0530493). The research involves developing an add-on to the current KMap evaluator tool. Figure 4 shows the options allowed by CLDT. The user will have the option of entering the design tool at any of the three phases shown. Each phase will have independent random problem statement generation as well as the ability to take the solution form the previous phase and assess the answers.

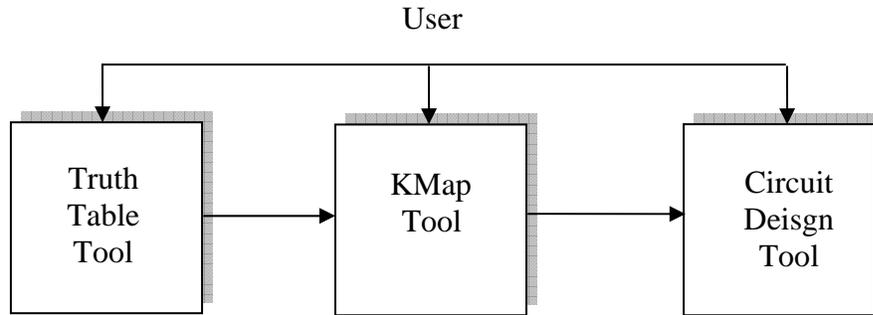


Figure 4: User tool option

3.1. The Truth Table Tool

The truth table portion of CLDT is designed to allow the user to choose the number of inputs and percentage of 'don't care' conditions for the truth table. The table is generated. The following portion of the CLDT tool is to allow the user to practice the transfer of truth tables into KMaps. The user first gets to decide how many cells are needed to generate a KMap for the given truth table. If the answer is incorrect the user is prompted for another answer. Once the user provides a correct response then the Map is generated and the user is now able to populate the map. The tool will allow for both the novice and expert user. For the novice user, the tool will allow the user to highlight (as shown in Figure 5) the output that will be used to populate the map. The user is then supposed to fill in the appropriate cell in the map. As soon as the answer is input, the tool will detect it and respond with a 'correct' or 'incorrect' prompt. The reason this methodology is used is to allow for the novice user to know step by step how they are doing in their design process. In the expert mode, the user is allowed to completely populate the KMap and then submit the answer for assessment.

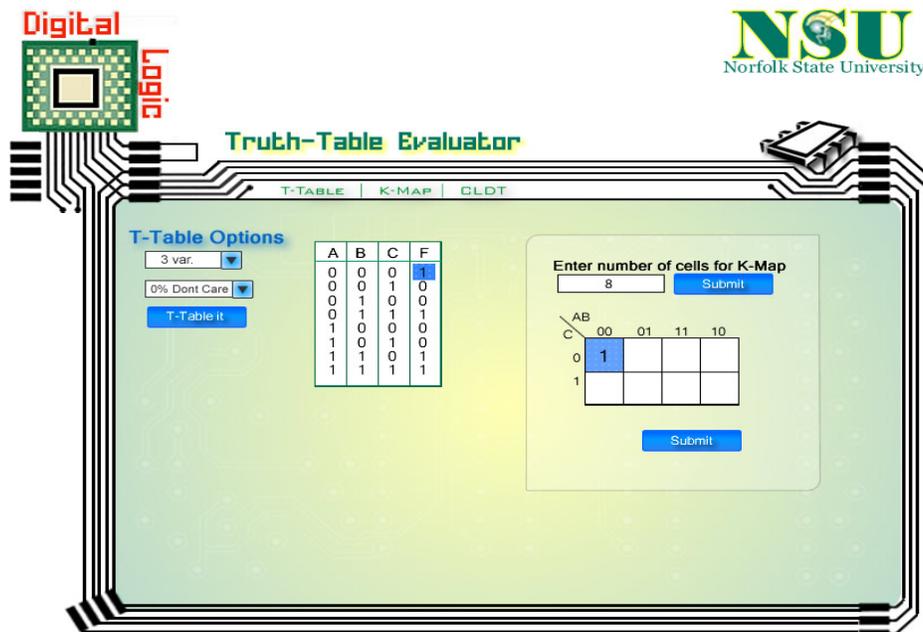


Figure 5: Design screenshot of the truth table phase of the CLDT tool

3.2. Current KMap Evaluator Tool

Morsi (2004) developed the Karnaugh Map Evaluator Tool. The primary function of this tool is to aid students studying digital logic in the understanding of Karnaugh maps and their ability to simplify switching functions. This tool provides an opportunity for students to practice minimization methods learned in the classroom. Students are presented with randomly generated Karnaugh maps and are required to create minimized expressions. The tool allows for both POS and SOP expressions. These minimized expressions are then verified to be correct and completely minimized by the software and the student is alerted accordingly. Figure 6 shows a screenshot of the current tool available at www.ece-edu.com.

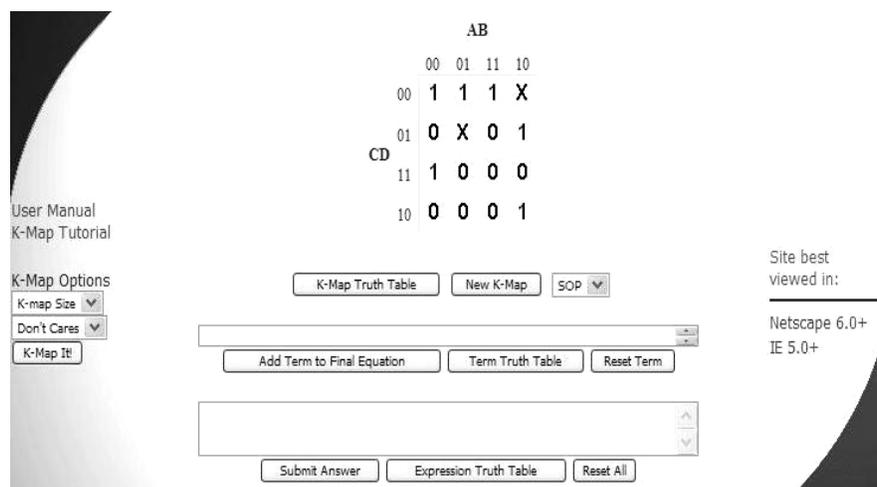


Figure 6: KMap evaluator tool screenshot

3.3. The Combinational Circuit Implementation Tool

This is the tail end add-on to the KMap evaluator tool. It will take the answer provided by the user from the KMap phase and allows the user to design the circuit using AND, OR, and NOT gates. The user will have the option on number of inputs to use on each gate. After the user has implemented the circuit the tool will assess the answer and prompt the user with a 'correct' or 'incorrect' response. Figure 7 shows the proposed design of the implementation tool.



Figure 7: Combinational circuit implementation tool

4. WORK IN PROGRESS STATUS

This project is an NSF funded project (EEC-0530493) that is to be completed in October 2006. At the time of writing this 'Work In Progress' paper, the design of the tool has been developed and the implementation of the truth table phase of the tool is underway. The tutorials and manuals as well as the circuit implementation phase of the tool are in the design phase and expected to be completed May 2006. The tool will be pilot tested with Engineering students at Norfolk State University in the Fall semester of 2006. It is intended that qualitative as well as quantitative assessment will be undertaken to view the full impact of this tool on students' learning.

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