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Reliability study of organic complementary logic inverters using constant voltage stress

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ABSTRACT

We performed constant voltage stresses with different bias conditions on all-organic complementary inverters. We found a 20% maximum variation of DC inverter parameters after a 10^4-s stress. However, the largest stress-induced degradation was found in the delay times, which increased by a factor as high as 7. This is mainly due to the threshold voltage variation of the p-type thin-film-transistor and the mobility reduction of the n-type thin-film transistors, which both decrease the saturation drain current.

1. Introduction

Progresses on Organic-Thin-Film-Transistors (OTFTs) made them a promising low-cost alternative to a-Si TFTs [1,2]. Organic devices have many advantages with respect to their silicon counterparts. In fact, organic materials can be inexpensively deposited using many techniques, such as spin-coating or ink-jet printing [3,4]. Those processes require much lower temperatures than those required for silicon deposition, allowing the growth of organic semiconductors over plastic substrates. Plastic substrates, in turn, are flexible, much lighter, more robust to mechanical deformation and cheaper than glass, allowing the integration of organic electronics in many fields. For instance, OTFTs could be employed in RF-IDs, flexible displays, smart textiles, sensors, etc. In many of these applications, a relatively low operating frequency is required, and they are mainly battery or near-field powered. The limited energy/power budget makes complementary logic a desirable choice to cut down power requirements, because static power dissipation is minimized, while dynamic power is relatively small, due to the low operating frequency. Complementary logic also features better noise margins, with respect to nMOS- or pMOS-only logic.

Unfortunately, OTFTs still have some drawbacks especially in terms of stability and reliability. In fact, OTFTs are very sensitive to air and humidity exposure [5,6], and their characteristics change under illumination, with bias and with temperature [7]. Many works in the literature have addressed the OTFT stability and reliability under electrical stress [7–12], light [7,11–13] and ultraviolet exposure [14–18].

Some works also already addressed the characterization of inverters with complementary OTFTs [19–21], or analyzed the bias effects on the DC inverter characteristics with only p-type or n-type OTFTs [22,23]. Very few works [24,25] also provided some results on bias effects on the DC characteristics of complementary inverters. However, our work represents the first systematic investigation of the reliability of inverters with all-organic complementary thin-film-transistors, using accelerated electrical stress. Our analysis not only includes the most important static OTFTs and inverter parameters, but also includes for the first time the propagation delay variation, never considered before in the reliability study of OTFT-based inverters.

2. Experimental and devices

Throughout this work, we analyzed complementary inverters with p-type and n-type OTFTs, whose cross section is shown in Fig. 1a. Devices were fabricated in Bottom Gate – Top Contact configuration, on glass substrates with gate contact consisting of a 150 nm thick ITO layer. A 450-nm Poly(methyl methacrylate) (PMMA) layer was spin-coated on top of ITO as dielectric layer. A 20-nm thick semiconductor layer was deposited by physical vapor deposition at 0.015 nm/s. The n-type and p-type layers were Diperfluorohexyl-Quaterthiophene (DFH-4T) and Dihexyl-Quaterthiophene (DH-4T), respectively [26]. Finally, 70-nm thick gold drain and source electrodes were deposited on top of the stack

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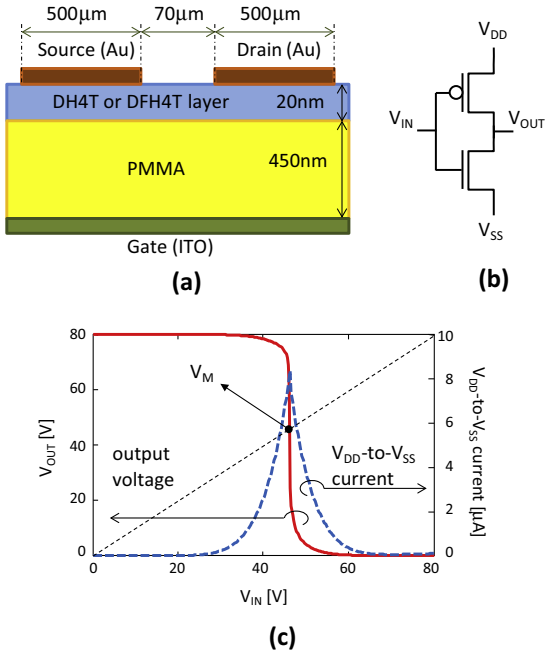

Fig. 1. (a) Cross section of n-channel (DFH4T) and p-channel (DH4T) organic TFT used in this work. (b) Inverter schematics with signal names, which will be used throughout this work. (c) Typical transfer characteristics (left scale) and direct path current (right scale) of the inverters used in this work.

at 0.1 nm/s. OTFTs' channel width was 12 mm, while channel length was 70 µm. The devices are encapsulated with glass covers, to avoid degradation due to air exposure. Electron mobility of the n-type OTFTs (nTFTs) is 0.28 $cm^2 V^{-1} s^{-1}$ and hole mobility of the p-type OTFTs (pTFTs) is 0.09 $cm^2 V^{-1} s^{-1}$, before stress.

The stress procedure consists of a Constant Voltage Stress (CVS), which is periodically interrupted to perform characterizations. The CVS is performed with different biases and connection, which are summarized in Table 1. Fig. 1b shows the inverter schematics with the signal naming conventions, which will be used in this work. The connections, named SH, SL, and SAT, emulate some of the different inverter operating conditions. In SH the inverter is stressed with the input held at the logic level high (nTFT is in the ON state, the pTFT is in the OFF state). In the SL configuration, the input is held at the logic level low (nTFT is in the OFF state, the pTFT is in the ON state). In SAT connection, the bias configuration is chosen so that both transistors are conducting the saturation current and each OTFT is stressed with $|V_{DS}| = |V_{GS}| = 100$ V. This particular configuration has been chosen to emulate the degradation, which occurs just after the rising and the falling edges of the input voltage, when the inverter is loaded with a large capacitance. In fact, when the input goes from "1" to "0", the nTFT will turn-off in a relatively short time. The pTFT also turns on, but, because of the large capacitive load, its V_{DS} will remain close to $-V_{DD}$, for a relatively long time, depending on the capacitive load. Consequently, the pTFT will be subjected for a relatively long time to a large $|V_{DS}|$ with $V_{GS} = -100$ V. A similar condition occurs on the nTFT during the "0" to "1" transition (of course, with opposite V_{GS} and V_{DS} polarities).

In SH and SL the power supply voltage is 100 V to accelerate the degradation. In SAT, the $|V_{DD} - V_{SS}|$ voltage is 200 V, but each transistor is stressed with $|V_{DS}| = |V_{GS}| = 100$ V.

Characterizations considered in this work include:

(1) The double-sweep saturation current–gate voltage curve (i.e. the I_D–V_{GS} taken with $V_{GS} = V_{DS}$, I_{SAT}–V_{GS} hereafter) of pTFTs and nTFTs.

Table 1
Stress conditions.

Signal	Stress configuration		
	SH	SL	SAT
V_{DD}	100 V	100 V	100 V
V_{SS}	0 V	100 V	−100 V
V_{in}	100 V	0 V	0 V
V_{OUT}	Open	Open	0 V

(2) The transfer characteristics (I_D–V_{GS}, with $|V_{DS}| = 1$ V).
(3) The double-sweep inverter transfer curve.
(4) The inverter transient step response (taken with a custom compensated 1 GΩ probe to minimize output loading).

A custom low-leakage switch matrix was also developed to allow for the single pTFT or nTFT characterization. Fig. 1c shows the static characteristics and the V_{DD}-to-V_{SS} current of one of the analyzed inverters.

The stress voltage was set to 100 V, in absolute value. Measurement voltage was limited to 80 V. It is worth to note that the voltages are remarkably high, because we are evaluating samples with high-thickness and low-k dielectrics. However, lower operating voltages are easily achievable employing thinner or high-k dielectrics. In a previous work on OTFTs subjected to CVS (see Ref. [27]), we found that, breakdowns apart, the PMMA layer degradation had a smaller impact on the characteristics compared to the degradation of the semiconductor layer. For this reason, in the present work we are focusing only on the effects of the organic semiconductor degradation on the inverter characteristics.

3. Results and discussions

This section is organized as follows: we first show and discuss the effects of electrical stresses at the transistor-level (Section 3.1), then we analyze the effects of OTFT degradation on the inverter characteristics (Section 3.2).

3.1. TFTs

In Fig. 2a–c, we show some selected I_{SAT}–V_{GS} curves measured during the CVS. Insets show a zoom of the curves, to appreciate the small hysteresis in the linear scale, which will be discussed later. In SH, there are very small variations in the pTFT and large degradation in the nTFT. For instance, the saturation drain current exhibit a 70% decrease in the nTFT and less than 10% decrease in the pTFT. The opposite occurs in SL: the pTFT degradation is larger than in nTFT (the saturation drain currents of the nTFT and pTFT decrease of 20% and 50%, respectively). In SAT, i.e. when both TFTs are driving current during stress, both TFTs feature the largest variations (the saturation drain currents decrease of 80% and 45% in nTFT and pTFT, respectively).

Using the trapped-charge-limited current model [28], from the I_{SAT}–V_{GS} and the I_D–V_{GS}, we calculated, the threshold voltage (V_{TH}), and the high electric field mobility (μ). From the subthreshold swing of the I_D–V_{GS} we evaluated the interface trap density variation (ΔN_{IT}).

Fig. 3a–c shows V_{TH}, μ (normalized to the initial value), and ΔN_{IT} evolutions during CVS, plotted as average between the values calculated from the forward and backward sweeps. The evolutions of these parameters suggest different degradation mechanisms in pTFTs and nTFTs, depending on the CVS connections. For instance, the nTFTs mostly exhibit a large μ reduction, especially in SH and SAT (up to 60%), accompanied by large ΔN_{IT} increase. In pTFTs, the parameters are almost unchanged in SH, and μ shows at most a

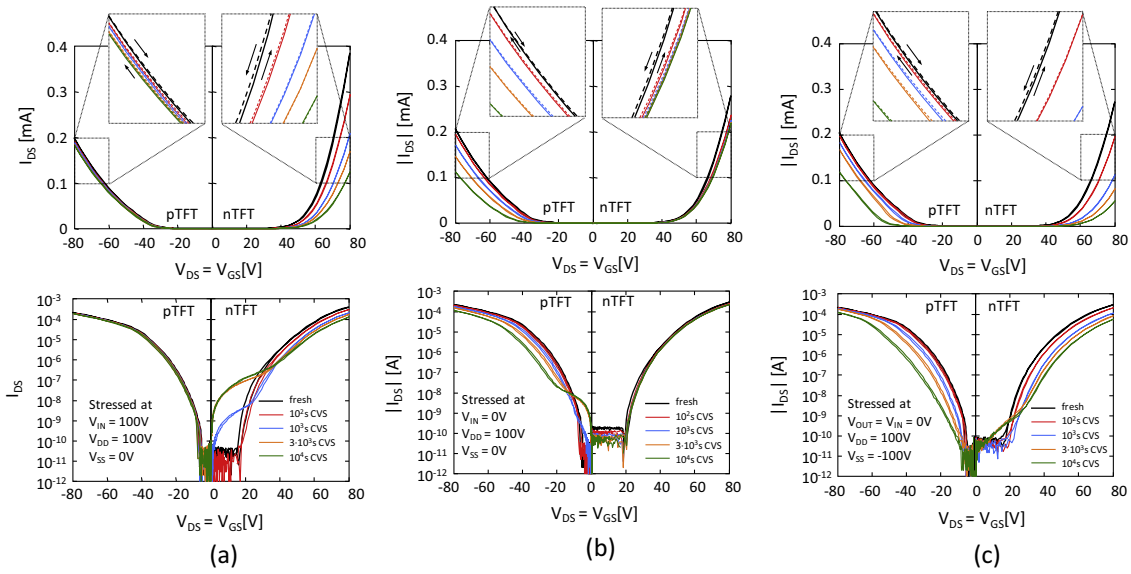

Fig. 2. I_D–V_{GS} curves taken with $V_{GS} = V_{DS}$ (I_{SAT}–V_{GS}) in the fresh device and after electrical stress for different stress configurations: (a) configuration SH (left column), (b) configuration SL (left column) and (c) configuration SAT (right column). Top plots are in linear scale, bottom plots are in log scale.

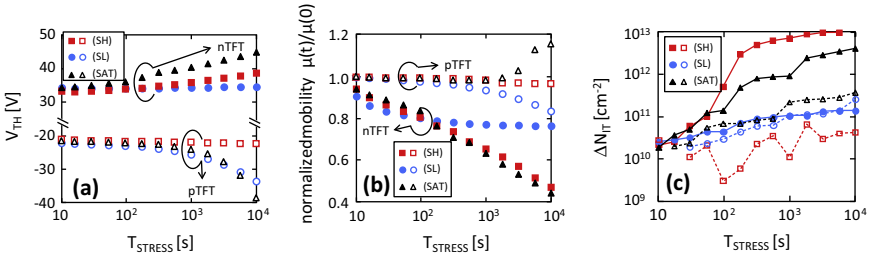

Fig. 3. Comparison of the evolution of some electrical parameters of nTFTs and pTFTs for different types of stress: (a) threshold voltage; (b) carrier mobility; (c) interface trap generation. pTFTs mainly show a V_{TH} shift, nTFTs mostly exhibit a mobility reduction. Interface trap generation is dominant in nTFT. The extents of V_{TH} and mobility variations strongly depend on the CVS configuration, and they are maximum in SAT, i.e. with nTFT and pTFT stressed in saturation region.

17% variation in SL and SAT. Moreover in, pTFTs, even ΔN_{IT} is smaller than in nTFTs (of 1 order of magnitude in SAT). Instead, the dominant degradation mechanism of pTFTs in SL and SAT is the V_{TH} decrease (as high as −12 V and −18 V, respectively). In nTFTs the V_{TH} variation has opposite sign and it is less pronounced with respect to pTFTs. In particular the V_{TH} variation is less than 1 V, 5 V and 10 V in SL, SH and SAT, respectively.

Data shown in Fig. 3a–c lead us to two immediate observations. First, the OTFTs are much more degraded in the ON-state (SH for nTFTs and SL for pTFTs) and even more in when they are also driving current (SAT). This is not unexpected, as, when the channel is formed, the degradation can take place in the whole channel area. Conversely, when the OTFT is OFF, the degradation can occur only on the drain side. As a second observation, the different ways the pTFTs and nTFTs degrade suggest a key role of the organic semiconductor materials in the TFT parameter degradation. This is in agreement with our previous findings reported in [27], where we demonstrated that the dielectric degradation has only a marginal contribution in the interface defect generation.

The negative V_{TH} variation of pTFTs comes from positive charge trapping, while the positive V_{TH} variation of nTFTs is due to negative charge trapping. The mobility reduction comes from the stress-induced semiconductor degradation, especially at the interface, as confirmed also by the larger interface trap density variation observed in nTFTs (see Fig. 3c). In other words, the main degradation phenomenon, which leads to the drain current decrease in the pTFT, is the positive charge trapping. On the other hand, the large mobility degradation is the main responsible for the drain current reduction of nTFTs. The positive V_{TH} variation also contributes to the further I_{SAT} reduction in nTFTs.

We believe that positive charge trapping on pTFTs occurs due to the strong hole injection in the PMMA layer from the semiconductor. In fact, during SL and SAT holes are injected from the channel and they are trapped in PMMA traps. In nTFTs, holes are much less efficiently injected in the PMMA during SH and SAT, because injection would occur directly from the ITO gate to PMMA with a higher energy barrier. In fact, ITO has a 4.9-eV work function, whereas the HOMO level of the DH4T is 5.8 eV below the vacuum level [29–31]. As a result, hole injection from the DH4T layer is much more favored, because the barrier height from DH4T and PMMA layer is 0.9 eV smaller than the barrier from ITO and PMMA. Similarly, during SH and SAT, electrons could be injected from the channel into the PMMA in nTFTs, explaining their initial V_{TH} increase.

Furthermore, during SH, only the region below the drain contact of the pTFT is stressed (being $V_{GS} = 0$ V), and the same occurs in the nTFT during SL. We believe that the drain region plays a minor role in the current flow, explaining why V_{TH} and μ, which are calculated from the saturation drain current, featured smaller variations on those OTFTs stressed in the OFF state. To confirm this idea, we carried out a 2D drift–diffusion simulation: the simulated current density at $V_{GS} = V_{DS} = 60$ V is shown in Fig. 4. From Fig. 4 we see that the current flow widely spreads below the source contact,

but it is very crowded in a narrow region at the edge of the drain contact, i.e. it does not appreciably flow *under* the drain contact, i.e., the region that was primarily subjected to stress in off-state conditions.

Given the same stress conditions, the nTFT exhibits the largest degradation, confirming that n-type organic semiconductors are much more sensitive to process-induced oxygen/moisture contaminants, due to the energetic levels, which favor oxidation and carrier trapping as often observed in several works (see for instance [32,33]).

3.2. Inverters

The OTFT degradation affects both the static and the dynamic behavior of the inverter. Fig. 5a–c shows the zooms around the switching threshold of the voltage-transfer-characteristics (VTC) of the inverter, taken during SH, SL and SAT stresses. The VTC has been measured by applying a double voltage sweep at the inverter input terminal, in order to monitor the hysteresis. These show different modifications, depending on the stress condition. For instance, during SH (Fig. 5a) the curve progressively shifts rightward, and the opposite occurs in SL (Fig. 5b). During SAT (Fig. 5c), the curve initially shifts rightward, then leftward. These curves also show a noticeable hysteresis, whose origin will be discussed later.

From these curves, we calculated the most relevant figures of merit describing the inverter static behavior, which are plotted in Fig. 6. Because of the hysteresis, these parameters are calculated both from the forward (i.e. when the input voltage sweeps from 0 V to 80 V) and the backward sweep (i.e. when the voltage sweeps from 80 V to 0 V). Instead, the output logic level does not depend on the sweep direction. The inverter threshold logic level (V_M on Fig. 6a) and the high and the low input logic levels (V_{IH} and V_{IL}, respectively, in Fig. 6b) increase in SH connection and they decreases in SL connection. This is due to the stronger degradation of the nTFTs in SH and the pTFTs in SL. In SAT, V_M, V_{IL}, and V_{IH}, exhibit a turn-around, mainly due to the combined degradation of nTFT (dominant at $T_{STRESS} < 300$ s) and pTFT (dominant at $T_{STRESS} > 300$ s). The output voltage logic values (V_{OH} and V_{OL}) exhibit appreciable variation only in SH connection, due to some small breakdowns localized at the drain contact. However, despite those breakdowns, occurred after 10^3 s, the inverters are still operational.

In Fig. 6e, we plot the inverter hysteresis width calculated as the difference between the V_M values in the forward and backward sweep ($V_{M,forward} - V_{M,backward}$). Such hysteresis remains below 3 V (i.e. less than 4% of V_{DD}) within the duration of the stress. The hysteresis width is comparable with the sum of the pTFT and nTFT hysteresis widths. However, another contribution should be taken into account, especially at the end of the SAT stress: the sum of the pTFT and nTFT threshold voltages, which becomes larger than V_{DD}. In this way, there is a region of the inverter VTC, in which none of the TFTs is in the ON state (or they are in a weak ON state, i.e. they can conduct only a very small current). In this region, the inverter's output is in a high-impedance state and the relatively large output capacitance keeps the output voltage, especially with fast VTC sweep rates. In this way, during the forward sweep, the pTFT turns-off earlier than the nTFT's turn-on, and the output remains high until the V_{TH} of the nTFT is not reached. On the backward sweep, the nTFT turns off and the output remains at a low level, until the pTFT turns-on.

Remarkably, the V_{TH} and μ variations of Fig. 3 affect the saturation drain current. However, since the stress affects (even though with different extent) both OTFTs, the variations compensate each other, with limited effects on the static inverter parameters, especially in SAT, even though SAT was the configuration in which we found the largest pTFT and nTFT degradations.

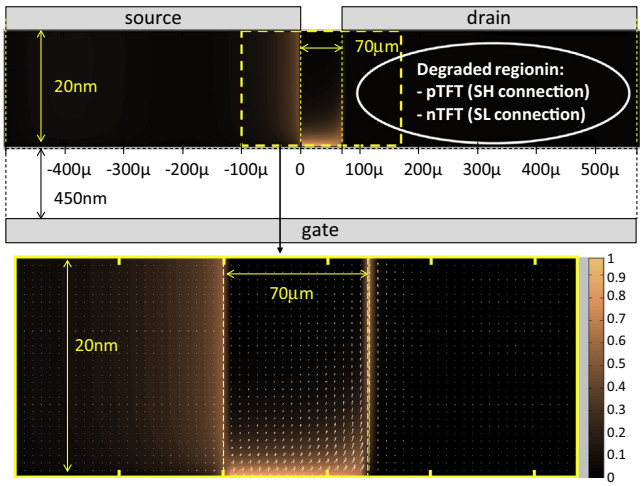

Fig. 4. 2D simulation of the current flow across the OTFT ($V_{GS} = V_{DS} = 60$ V). The color scale represents the current intensity in A.U. Noticeably, the saturation current spreads out on the source and channel regions, but current crowding occurs at the drain contact edge.

Instead, the most important variations occur on the dynamic behavior, shown in Figs. 7 and 8. In fact, during the H → L transitions, the nTFT operates, at least initially, in the saturation region. Similarly, during the L → H transition, the pTFT initially operates in the saturation region. Hence, because the saturation drain current decreases, the propagation delay increases. The effects are larger on the fall time (t_f) and on the high-to-low propagation time (t_{pHL}), i.e. those times controlled by the nTFT (see Fig. 8). In fact, while the rise time (t_r) and low-to-high propagation time (t_{pLH}) both increase by a factor ≈2, t_f and t_{pHL} increase by a factor 7 and 5, respectively. This is not surprising, as the nTFT shows the larger current variation. Remarkably, the switching time variations are well correlated with the saturation drain current reduction, as expected.

At this point, some considerations are worth to be drawn. First, the complementary configuration of the inverter partially mitigates the stress induced DC characteristics variation of the OTFTs. However, this mitigation is mostly effective only when the inverter is driven with a square wave having a duty cycle close to 50%, i.e. when it spends half of its time at the logic output low and half of its time at the logic output high. Breakdowns induce leakages, which not only can change the output high or low logic voltage level, but also they can strongly increase the static power dissipation. Moreover, such breakdowns might act as a resistive loading of the logic gate, which drives the inverter's input, further reducing the effective noise margins. However, despite these breakdowns, the inverter is still operational thanks also to the high noise margins of the complementary logic approach.

A second remark is related to the switching speeds. In fact, while after a substantial accelerated stress time the inverter is still operational from the static viewpoint, the switching times strongly increase by a factor as high as 5 and 7, in the propagation and transition times, respectively. This could be a serious concern because the designer should take into account that the speed of the gates will progressively reduce during the device lifetime. Furthermore, a large rise or fall time could be detrimental in sequential logic, where a sharp edge transition might be required, for instance in some edge triggered flip-flop configurations. Furthermore, the large variation on the propagation delays severely impacts some circuits, such as ring oscillators, where the oscillation frequency is proportional to the propagation delays themselves. For instance, if the inverters used in this work would be employed in a ring

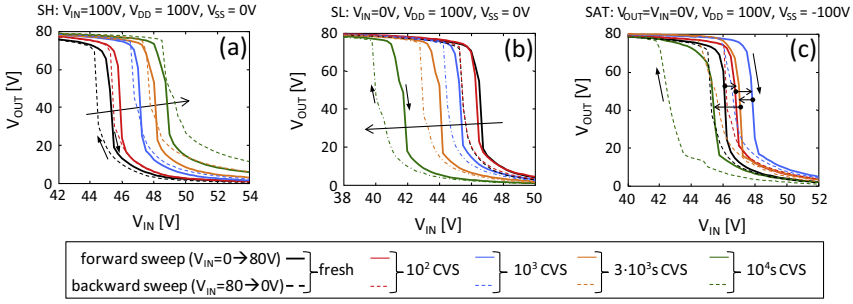

Fig. 5. Zoom of the inverter voltage transfer characteristics, around the logic threshold voltage. In SH (a), the curves progressively shift rightward. In SL (b), the shift is leftward. In SAT (c), the shift initially is rightward, then it becomes leftward. Forward sweeps are shown with solid lines, backward sweeps are shown with dashed lines.

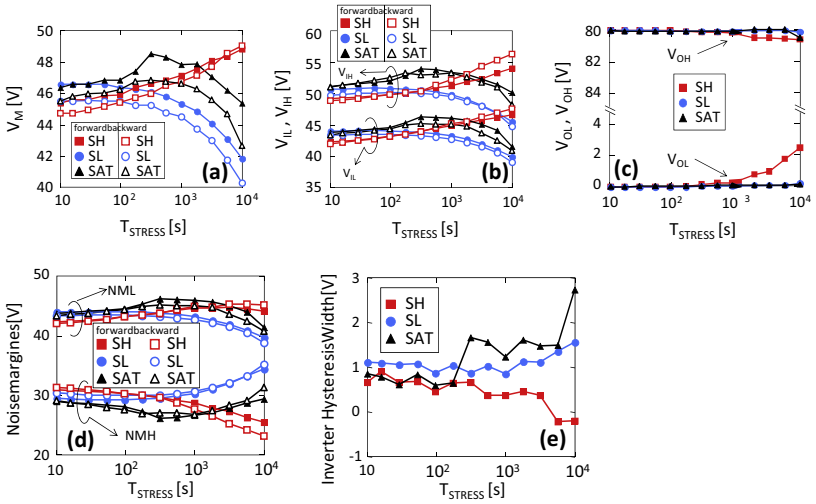

Fig. 6. Evolution of the most important inverter static parameters during the three types of stress: (a) logic threshold voltage, V_M; (b) logic low and high input voltage value, V_{IL} and V_{IH} (c) logic low and high output voltage value, V_{OL} and V_{OH}; (d) low and high level noise margins, NM_L and NM_H. (e) Hysteresis width, calculated as the difference $V_{M,forward} - V_{M,backward}$.

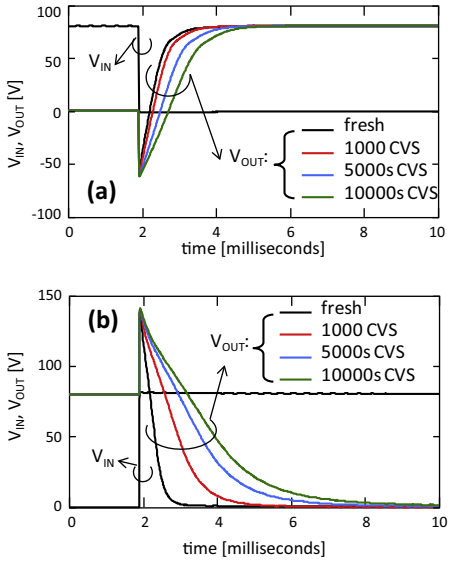

Fig. 7. Inverter output transients during the low-to-high level (a) and high-to-low level (b) commutations.

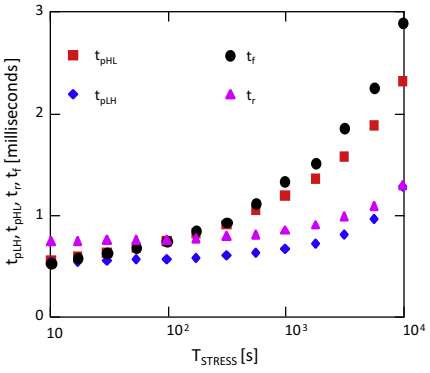

Fig. 8. Evolution of the propagation delays, the rise time, and the fall time of the inverter output signal (stress has been carried out with SAT connection). t_{pHL} and t_f exhibit the larger variations (×5 and ×7, respectively), being determined only by the nTFT, which shows the larger saturation current decrease at $V_{GS} = V_{DS} = 80$ V (see Fig. 2c).

oscillator configuration, the frequency would decrease by a factor 3.5, which could be unacceptable. Therefore proper countermeasures should be employed to take into account the noticeable frequency reduction induced by stress.

Several other issues still remain open. For instance, the actual effects of stress-induced degradation in more complex circuitry such as multiple-input gates, flip-flops, and ring oscillators have not been addressed yet. Furthermore, pulsed stress could better emulate the inverter operation, with respect to a simple constant voltage stress. These and other issues need to be fully addressed, for a comprehensive view of the scenario on the degradation of organic thin-film-transistor based circuitry.

4. Conclusions

We subjected all-organic complementary logic inverters to constant voltage stress, analyzing the static characteristics of the p- and n-type thin-film-transistors and, for the first time, not only the static but also the dynamic characteristics of the inverter.

The constant voltage stress configurations were chosen to emulate different inverter operating conditions. Large variations were observed on the electrical characteristics of the OTFT, which was in the ON state during the stress (up to −80% on some parameters such as the saturation drain current). Smaller variations were observed in the OFF state transistor. Despite the large variations in the electrical characteristics of the OTFTs, the inverter static characteristics were much less affected, especially when both transistors are stressed at the same time. However, we found that much stronger variations were measured in the inverter delay times, which increased by a factor up to 7. This may become an issue much more crucial than the degradation of static characteristics, and it must be taken into account at design level.

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