A Comprehensive Compact SCR Model for CDM ESD Circuit Simulation

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I. Introduction

The increased usage of automated manufacturing and testing equipment has led to environments that are more likely to have the presence of the charge device model (CDM) ESD, rather than the more well-known human body model (HBM). CDM events can easily reach several Amps within 1 ns and are accompanied by damped but fast oscillations, which makes the development of an accurate and compact model for CDM ESD devices very difficult. Silicon controlled rectifier (SCR) has long been used as a robust and area-efficient on-chip ESD protection device, but an SCR compact model for CDM ESD applications is not widely available. Juliano and Rosenbaum developed a model based on the Verilog-A coded behavior modeling to describe the SCR snapback [1], but a smoothing function has to be used to ensure continuity. Other SCR compact models built from a macromodel consisting of existing device models were intended for transmission line pulsing (TLP) or HBM responses and are not applicable for the simulation of circuits subject to the CDM stress [2]-[4]. In this paper, we seek to develop a comprehensive and accurate compact model for a high-holding, low-voltage triggering SCR (HH-LVTSCR) [5], with special attentions given to accurately modeling the CDM-relevant operation states in order to simulate the response of complete I/O circuits under CDM stresses.

II. Compact Model Development

When the SCR device is integrated with the core circuit to perform ESD protection, the anode is tied to pad and the cathode to the ground bus, as shown in Fig. 1. The cross section and the terminal connection of a HH-LVTSCR are shown in Fig. 2(a). Macromodeling will be used in this work, as it is highly suitable for modeling such a device having a complex structure that is difficult to describe with closed-form analytical equations.

During the CDM event, if the substrate of the device is negatively charged and the anode is grounded, the HH-LVTSCR will trigger in the positive operation and result in snapback. On the other hand, if the substrate of the SCR is positively charged and the anode is grounded, then the p-substrate/n-well junction is forward biased and current flows through the forward biased junction. Since the emitter-NPN and p-well terminals are also tied to the substrate, the current will also pass through the forward biased p-well/n-well junction. Thus, in addition to the basic components of the NPN and PNP bipolar transistors and a MOSFET, a diode, D_{sub}, a parasitic PNP transistor, and two substrate resistances, $R_{N\text{-Well-2}}$ and R_{sub}, need to be included in the SCR macromodel, as shown in Fig. 2(b). In the macromodel, the PNP transistor, NPN transistor and NMOS are described by the Gummel-Poon (GP), VBIC and BSIM3v3 models, respectively. Fig. 3 shows detailed equivalent circuit including the GP, VBIC, and BSIM models, as well as the parasitic BJT, diode and resistors. The GP model is normally sufficiently accurate for the PNP BJT. The reason for using the VBIC model for the NPN BJT is that it is more advanced and comprehensive than the conventional GP model, and the parasitic PNP transistor has been built into VBIC model with the algorithms for the correlation between the primary NPN and the parasitic PNP transistors fine-tuned.

Oscillatory nature of CDM stress requires the macromodel to be able to describe the characteristic of the SCR device in negative operation. We have found that, if the GP model is used for the NPN transistor, the simulation results cannot fit the TLP measurement data since the coupled GP P/N/P and N/P/N BJT models cannot function correctly as a forward biased diode under the reverse bias. By using the macromodel scheme in Fig. 3, no extra diode is needed to model the negative characteristic.

III. Results and Discussions

HH-LVTSCR devices with a width of 100μm were fabricated in a 0.35-μm/3.3-V fully salicided BiCMOS process for model extraction and TLP measurement. Fig. 4(a) shows an excellent match between the measured and simulated TLP I-V characteristic for both the forward and reverse directions. Fig. 4(b) and 4(c) compare the measured and simulated transient responses of the TLP voltage and current, respectively, in the SCR right after the triggering point. The pad voltage reaches a peak value of 9.42 V (trigger voltage) and then is decreased to 5.11 V (holding voltage) before it is turned off. The pad current, on the other hand, reaches a maximum value of 218 mA after the device turns on.

The HH-LVTSCR devices were integrated into SPDT analog switch parts with a package of 10-lead MicroPAK for the CDM test. The test results revealed that, with the SCR protecting devices at the pins, the input pins failed after a 500 V CDM zap and the output pins passed 1 kV CDM. The macromodel was implemented into the industry standard Cadence SPICE to simulate the response of the input and output pins under the CDM stresses. The NMOS in output buffer for pull-down has the snapback modeling capability. A calibrated the RLC circuit has been developed to generate the CDM pulses.

Fig. 5 shows the simulated transient voltage and current characteristics of the input pin subjecting to a positive 500 V CDM stress (i.e., negative substrate charging). The maximum voltage at the input pad, which is also the maximum voltage stressed at the gate oxide of the input MOS, is as high as 35 V, which caused the gate oxide failure. This may stem from that fact that the HH-LVTCSR does not trigger fast enough to discharge the CDM stress current, as evidenced by the current waveform lagging the voltage waveform during the positive portion of the first cycle. In the negative portion of the first cycle, the maximum voltage is much lower because the current will discharge through the forward-biased p-substrate/n-well and p-well/n-well junction diodes. The diodes can turn on quickly enough to safely shunt the current.

Fig. 6 shows the simulated transient voltage and current characteristics of the output pin subjecting to a positive 1 kV CDM stress. The output driver of the I/O circuits is self protecting, i.e., it operates in snapback mode during ESD tress, and thus it can supply an additional path to discharge the ESD current. The peak pad voltage is 24.4 V, which is much lower than that for the case of 500 V CDM on the input pin. In addition, there is no gate oxide at the output pin subjecting to the ESD stress. As such, the CDM robustness of the output pin is higher than that of the input pin. This is consistent with the experimental results showing that the input pins failed after a 500 V CDM zap whereas the output pins passed 1 kV CDM.

V. Conclusion

We have presented a comprehensive SCR compact model for CDM simulation. The work illustrated the useful and effective macromodeling approach of integrating the various industry standard models to describe the different devices imbedded in the SCR and treating the CDM-relevant operation states. In additional to the prediction of TLP results, the presented model demonstrates the effectiveness in analyzing CDM response of the I/O circuits and successfully explains why the input pins have lower CDM robustness than the output pins.

References

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Fig. 1 Schematic of on-chip ESD protection realized with SCR devices, showing the discharge current paths of different CDM zaps.

Fig. 2. (a) Cross-section view of the HH-LVTSCR. (b) Equivalent circuit of the HH-LVTSCR macromodel.

Fig. 4. (a) Simulated and measured TLP I-V characteristics of the HH-LVTSCR. (b) Simulated and measured time-dependent pad voltages and (c) pad currents right after the SCR triggering.

Fig. 3. Schematic of the HH-LVTSCR macromodel, showing the detailed connections of all internal nodes.

Fig. 5. Simulated transient voltage and current at the input pin under a positive 500 V CDM stress.

Fig. 6. Simulated transient voltage and currents at the output pin under a positive 1 kV CDM stress.