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Low-voltage bulk-driven rectifier for biomedical applications

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ABSTRACT

This paper introduces the novel design of a low-voltage low-power voltage rectifier based on bulk-driven (BD) winner-take-all (WTA) circuit. The proposed circuit is able to work as a half- or full-wave rectifier and it is specifically designed for battery-powered implantable and wearable medical devices. The main attractive features of the proposed circuit are topology simplicity, minimal number of transistors, accuracy and capability of rectifying signals with a relatively wide range of frequencies and amplitudes. The circuit was designed with single voltage supply of 0.6 V and consumes about 2.14 μW. Detailed simulations using TSMC 0.18 μm n-well CMOS technology were performed to prove the functionality and to fully characterize the circuit performance.

1. Introduction

During last decades the specific implementations of analog integrated circuits in the area of biomedical applications have become very attractive [1,2]. Applications such as implantable wearable electronics [3], physiological process monitoring [4], neural recording [5] and medical imaging systems [6] are among the most important. One of the most essential requirements of such circuits is the need of extremely low-voltage (LV) supply, low-power (LP) consumption [1–6] and the small size.

Many of the aforementioned applications are portable and require small battery size and lightweight with prolonged lifetime. As the device's gate oxide thickness and dimensions of state-of-the-art of CMOS decrease, it results in improvement of the speed and shrinking of the circuits' area of digital systems, the supply voltage must be decreased for reliability issues [7]. For analog circuits the continuous decreasing of the supply voltage and the relatively high threshold voltages are the main limitations regarding the LV design. The threshold voltage remains at relatively high level compared to the supply voltages in order to minimize the leakages which is one of the main drawbacks in modern processes. Therefore, non-conventional analog design topologies suitable for operation under LV and LP environments must be invented.

The voltage rectifier with LV LP capabilities is one of the basic blocks that is necessary in a variety of wearable biomedical electronics systems which are used for real time processing of biological signals [8]. Such biological signal could be generated by bionic implants [9], neural recording systems [10], surface electromyography systems [11] and artificial feedback and management systems [12]. Several LV LP rectifiers for biomedical applications were proposed in the literature [13–18].

The known approach for voltage rectifiers is based on winner-take-all (WTA) circuit, which was firstly presented in [19]. Many WTA circuits were employed in the implementation of current-mode [20] and voltage-mode rectifiers [21,44]. However, these rectifiers are not suitable for biomedical applications since they need extremely LV and LP conditions.

Non-conventional design techniques as bulk-driven [22,35], floating-gate and quasi-floating-gate [36–41] were introduced to reduce or even to remove the threshold voltage requirements from the signal path. The bulk-driven technique was first presented in [22] and many low-voltage active building blocks were designed based on this technique, such as voltage followers [23,24], op-amps [25,26], operational transconductance amplifiers (OTAs) [27–31], second generation current conveyor (CCII) [32,35], current differencing external transconductance amplifier (CDeTA) [33] and differential-input buffered and external transconductance amplifier (DBeTA) [34]. The main advantage of the aforementioned building blocks is the high input common-mode range since the input signal is applied to the bulk terminal of the input devices [22–35].

The main limitation of the bulk-driven technique is small bulk transconductance which is 3 to 5 times smaller than the corresponding gate-transconductance. Consequently, a relatively large input-referred noise occurred compared to the input-referred noise of gate-driven MOS devices [25,26,34]. Also, due to smaller bulk transconductance and larger input capacitance of the BD

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transistor in comparison to the gate-driven one the unity gain frequency of the BD technique is degraded [34]. Despite the fact that the BD technique comes with several limitations it has proven applicability in many LV LP applications, particularly battery-powered implantable and wearable medical devices. As recognized fact these devices process biological signals and their characteristics are low amplitudes and low frequencies, i.e., they vary from a fraction of a hertz to several kilohertz with amplitude in range of micro up to millivolts. Furthermore, the low bulk transconductance is appreciated and requested in specific applications, for example to achieve low cut-off frequency of G_m–C low-pass filter, as in [31].

In this work, we propose a novel LV LP voltage rectifier which takes the advantages of the WTA circuit and bulk-driven technique. The main advantages of the proposed solution are: simplicity of the circuit structure, capabilities to work under LV LP conditions and the circuit can works as half- or full-wave rectifier by adding a simple inverter.

The paper is organized as follows. In Section 2, the bulk-driven and the WTA operation principles are presented. Section 3 describes the half- and full-wave operation and simulation results along with their evaluations are included in Section 4. Finally, Section 5 concludes the paper.

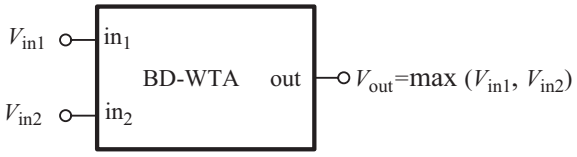

Fig. 1. BD-WTA symbol.

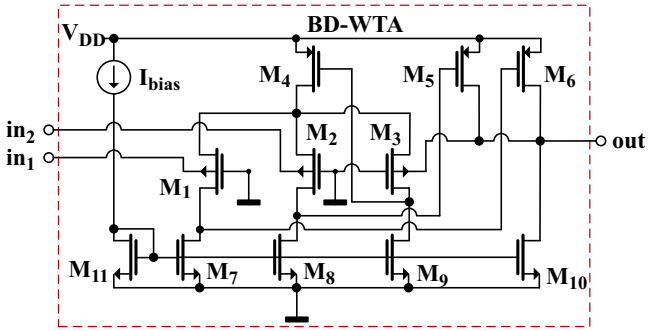

Fig. 2. Novel CMOS structure of BD-WTA circuit.

2. LV LP WTA based on bulk-driven technique

2.1. Bulk-driven principle

The drain current of a pMOS device which operates in weak-inversion, neglecting the channel length modulation, is given by:

$$I_D = I_{Do} e^{\frac{V_{GS}}{nU_t}} e^{\frac{n-1}{n}\frac{V_{BS}}{U_t}} \tag{1}$$

where I_{Do} is the drain current for $V_{GS}=V_{BS}=0$ and is proportional to the transistor aspect ratio, V_{GS} and V_{BS} is the gate-source and bulk-source voltages, respectively. The slope factor n is given by:

$$n = 1 + \frac{C_D}{C_{ox}} \tag{2}$$

where C_D is the depletion capacitance and C_{ox} the gate oxide capacitance. Based on Eq. (1), the bulk-transconductance g_{mb} of the pMOS device is given by the next expression:

$$g_{mb} = \frac{n-1}{n}\frac{I_D}{U_t} = \frac{n-1}{n} g_m \tag{3}$$

where g_m is the corresponding gate-transconductance of the same device biased under the same condition. The factor $(n-1)/n$ in Eq. (3) features strong dependency from fabrication process and temperature with values ranging between 0.2 and 0.4. Thus, the bulk- transconductance is expected to be less than the gate-driven transconductance [25,26,34]. On the other hand the main benefit of the bulk-driven technique is the extended input common mode range in many circuits like op-amps [25,26], OTAs [27–31], and CCIIs [32,35].

2.2. Circuit description of the bulk driven WTA circuit

The symbol of the proposed bulk-driven WTA circuit (BD-WTA) with two inputs and one output is shown in Fig. 1. The voltage output is equal to maximum input voltage.

The novel topology of the BD-WTA circuit is presented in Fig. 2. The input signals V_{in1} and V_{in2} are applied to the bulk terminals of transistors M_1 and M_2, respectively. Therefore, the input impedances of the input terminals in_1, in_2 are very high, because the bulks of the MOS transistors are used as the inputs of BD-WTA. Transistors M_{11}, M_7, M_8, M_9 and M_{10} act as a multiple output current mirror applying the constant current source I_{bias} to each branch of the circuit.

The circuit topology can be divided into two identical two-stage amplifiers. The first one constructed by M_1, M_3, M_4, M_7, M_9, M_6 and M_{10} where M_1, M_3, M_4 form the input stage, M_7–M_9 is the active load of the first stage while M_6, M_{10} is the second stage performing an extra voltage amplification. The input stages of both amplifiers constructed by a bulk-driven pMOS differential pair which is biased using a flipped voltage follower. The second one amplifier is formed by M_2, M_3, M_4, M_8, M_9, M_5 and M_{10}, where M_2, M_3, M_4 is the input stage, M_8–M_9 is the active load of the first stage and M_5–M_{10} is the second amplification stage. Transistor M_4 which acts as the tail current source belongs to both input stage. Also, it is obvious that both amplifiers share transistor M_3 which belongs to both differential pairs M_1–M_3 and M_2–M_3 while the output voltage is fed-back to its bulk terminal. Therefore, both amplifiers are connected in unity buffer configuration and each of them tries to implement the output voltage equal to their input voltage.

Based on the aforementioned assumptions the first amplifier handles the input V_{in1} and the second one handles the input V_{in2}. In order to explain the operation the WTA circuit let us suppose that $V_{in1} > V_{in2}$. For this case the drain current of M_2 is higher than the drain current of M_1 and thus the drain voltage of M_2 is much higher than the drain voltage of M_1 because of the voltage amplification of the first stage. Consequently, at the output stage, the gate voltage of M_5 will be much higher than the gate voltage of M_6. Therefore, the drain current of the current source transistor M_{10} will flow through transistor M_6 which in its turn means that only the first on amplifier will be active. Thus, the output voltage will follow V_{in1} which is the maximum input between the two inputs. In case $V_{in1} < V_{in2}$ then, following the same consideration, the output voltage will follow the input V_{in2}. It should be noted here than since the each amplifier includes two amplification stages the BD-WTA circuit is able to distinguish small input differences.

A straightforward analysis of a small-signal equivalent circuit brings the following expressions for the voltage transfer ratio β_{01} and β_{02}:

When $V_{in1} > V_{in2}$ then

$$\beta_{01} = \frac{V_{out}}{V_{in1}} = \frac{g_{mb,M1}\, r_{out01}\, g_{m,M6}\, r_{out2}}{1 + g_{mb,M3}\, r_{out01}\, g_{m,M6}\, r_{out2}} \approx \frac{g_{mb,+1}}{g_{mb,M3}} \approx 1 \tag{4}$$

when $V_{in2} > V_{in1}$ then:

$$\beta_{02} = \frac{V_{out}}{V_{in2}} = \frac{g_{mb,M2}\, r_{out02}\, g_{m,M5}\, r_{out2}}{1 + g_{mb,M3}\, r_{out02}\, g_{m,M5}\, r_{out2}} \approx \frac{g_{mb,M2}}{g_{mb,M3}} \approx 1 \quad (5)$$

where g_m and g_{mb} denote the gate and bulk transconductances of the MOS devices, respectively, e.g. $g_{mb,M1}$ is the bulk transconductance of M_1. It should be mentioned here that r_{out2} is the output resistance of the second stages and r_{out01}, r_{out02} are the output resistances of the first stages which are formed by the group of transistors: M_1, M_3, M_4, M_7, M_9 and M_2, M_3, M_4, M_8, M_9, respectively.

Thanks to the negative feedback the low impedance value of the out terminal is guaranteed and it is given by:

$$R_{out} \approx \frac{1}{g_{mb,M1} r_{out01} g_{m,M6}} \| \frac{1}{g_{mb,M2} r_{out02} g_{m,M5}} \quad (6)$$

It is obvious that the proposed circuit offers high input and low output impedances that are important requirements for the voltage-mode operation.

The advantage of using a flipped voltage follower for the input stage biasing against the tail current transistor of the conventional bulk-driven input stage is the capability for operation under lower supply voltage [32]. Based on Fig. 2, the most critical path, regarding the minimum supply voltage, is formed by the stacked transistors M_4 and M_9. Therefore, the minimum supply $V_{DD.min}$ will be given by:

$$V_{DD.min} = V_{GS,M4} + V_{DS,M9} \quad (7)$$

where $V_{GS,M4}$ is the gate-source voltage of M_4 and $V_{DS,M9}$ is the drain- source voltage of the active load device M_9. The proposed WTA-BD circuit is more efficient regarding the minimum supply requirement compared with conventional bulk-driven input stages achieving the same common-mode dynamic range.

3. LV LP rectifier based on BD WTA

Fig. 3(a) shows the half-wave rectifier based on BD-WTA circuit. At the input in_1 the sinusoidal signal $V_{in1} = V_{bias} + V_m \sin \omega t$ is applied and at the input in_2 only the constant voltage V_{bias} is applied, where V_m is the input amplitude. For maximum input swing the voltage V_{bias} can be chosen equal $V_{DD}/2$. Therefore, the sinusoidal signal $V_{in1} = V_{bias} + V_m \sin \omega t$ is compared with the V_{bias} one, and the output voltage will be given by:

$$V_{out} = \begin{cases} V_{in1} = V_{bias} + V_m \sin \omega t, & V_{in1} > V_{bias} \\ V_{bias}, & V_{in1} \le V_{bias} \end{cases} \quad (8)$$

So, for positive half-wave $V_{out} = V_{in1}$ and or negative half-wave $V_{in1} < V_{bias}$ then $V_{out} = V_{bias}$. Hence a half-wave rectifier is obtained.

Fig. 3(b) shows the circuit topology of the full-wave rectifier, which consist of BD-WTA with bias circuit and a simple MOS inverter. The circuit of a simple analog inverter is presented in Fig. 4. The sinusoidal signal $V_{in1} = V_{bias} + V_m \sin \omega t$still applied to input in_1 and to the input in_{inv} of the simple inverter. The inverted sinusoidal signal of the V_{in1} is obtained from the output of the simple inverter (out_{inv}) and therefore the input signals of the BD-WTA circuit standalone will be $V_{in2} = -V_{in1}$. It should be noted here that the constant voltage which is appeared at the output of the inverter is adjusted to be equal to V_{bias} by appropriate selection of the aspect ratio of M_{12} and M_{13}. The output voltage is expected to be given by:

$$V_{out} = \begin{cases} V_{bias} + V_m \sin \omega t, & V_{in1} > V_{in2} \\ V_{bias} + V_m \sin \omega t, & V_{in1} \le V_{in2} \end{cases} \quad (9)$$

Then, for positive half-wave $V_{out} = V_{in1}$ and for negative half-wave $V_{in2} > V_{bias}$ then $V_{out} = V_{in2}$. Hence a full-wave rectifier is obtained.

4. Simulation results

The circuits were designed and simulated using TSMC 0.18 μm n-well CMOS process with single supply of 0.6 V. The used SPICE model is available on [42]. The bias voltage V_{bias} was 0.3 V (mid supply) and the power consumption was 2.14 μW. The optimal transistor aspect ratios and the bias components are given in Table 1.

The DC transfer characteristic of the simple inverter of Fig. 4 is shown in Fig. 5. For input voltage range from 100 to 500 mV the voltage error is below 4 mV, out of this range this error is dramatically increased. Therefore, using $V_{bias} = 0.3$ V and maximum input amplitude $V_{m.max}$ of 200 mV, the inverter is not expected to have strong impact to the overall rectifier accuracy.

Fig. 6 shows the DC transfer characteristic of BD-WTA rectifier in comparison with the ideal one and it confirms the precise rectification for input amplitude ranging 200 mV. The voltage offset is only 0.026 mV, and the large-signal positive and negative slopes of the characteristic are 0.997 and 0.994, respectively. It should be noted here that the difference between two characteristic for V_{in} below 100 mV is due to the limitation of the simple inverter.

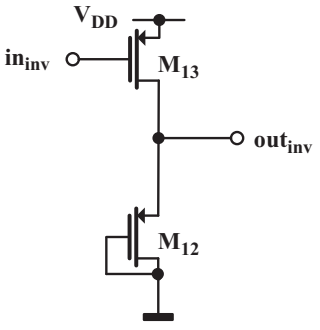

Fig. 4. Simple MOS Inverter.

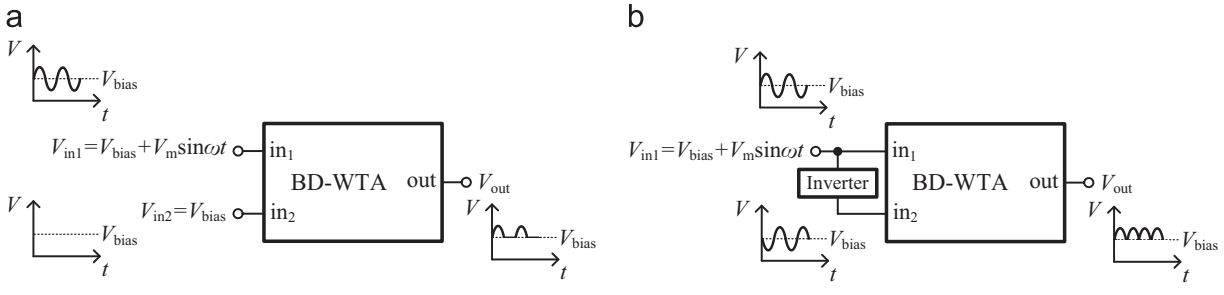

Fig. 3. BD-WTA half-wave (a) and full-wave rectifier (b).

Table 1
Component values and transistor aspect ratios from Figs. 2 and 4.

BD-WTA	W/L [μm/μm]
M_1, M_2, M_3	30/2
M_4	30/0.3
M_5, M_6	10/0.3
M_7, M_8, M_9, M_{11}	4/3
M_{10}	8/3
M_{12}, M_{13}	10/2
C_{load}=5 pF	
I_{bias}=0.6 μA	
V_{DD}=0.6 V	
V_{bias}=0.3 V	

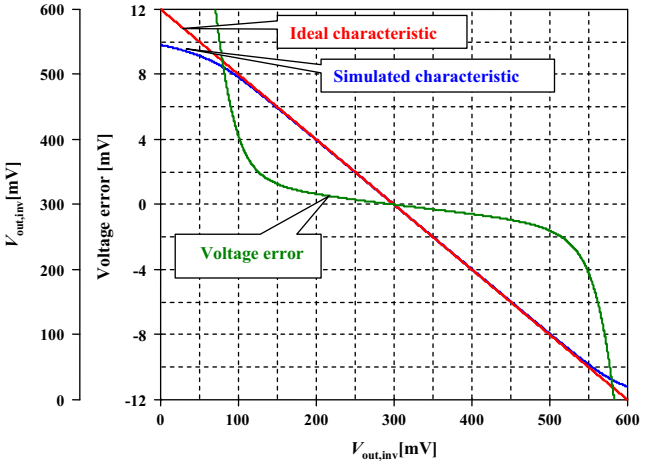

Fig. 5. DC transfer characteristic and voltage error of the simple analog inverter of Fig. 4.

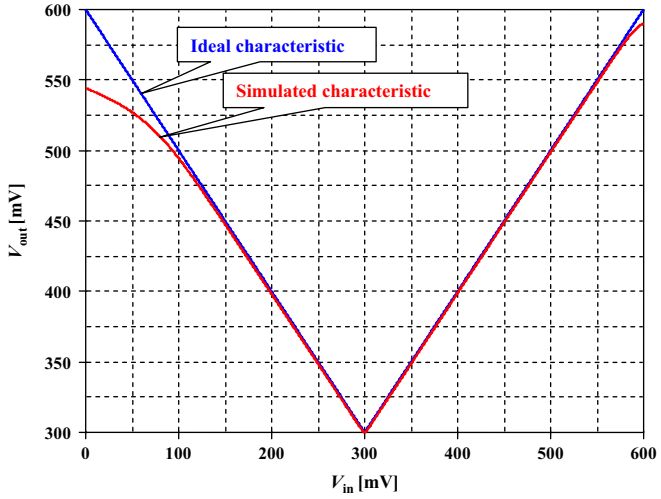

Fig. 6. DC transfer characteristic of BD-WTA full-wave rectifier.

The transistors threshold voltage changes due to process variation is the most critical circuit parameter which could have impact on circuit precision. Therefore, Monte Carlo analysis of the DC transfer characteristic with 10% variations of the transistors threshold voltage was performed. The results of Monte Carlo analysis, using 100 runs, are shown in Fig. 7, and confirm the reliability of circuit functionality. It should be mentioned that for input amplitude 200 mV the DC transfer characteristic remains almost unchangeable. Temperature analysis of the DC transfer characteristic with temperature in range of −10–90 °C where provided, and the simulation shows an overlapped curves, confirming a good temperatures stability of the proposed circuit.

Fig. 8 shows the transient responses of the input and output waveforms. The input signal was set with amplitude of 100 mV and frequency of 1 kHz and the load capacitor C_{load} was set to 5 pF.

It is noteworthy that with increasing the frequency and decreasing the amplitude of the input signal the capability of the rectifier to properly rectify the signal is declined. Therefore evaluation of the rectifier with various amplitudes and various frequencies must be done to determine the maximum frequency and minimum amplitude allowable of the input signal.

Fig. 9 shows the transient response of the output waveforms for input signal of 1 kHz and amplitudes from 25 mV to 125 mV with step of 25 mV. It is obvious here that the rectifier is capable to rectify a wide range of amplitudes.

Fig. 10 shows the transient responses of the input and output waveforms with amplitude 100 mV and frequency 10 kHz and 100 kHz. It is apparent the good functionality of the rectifier with 10 kHz input signal whereas the distortion of the output signal appears with 100 kHz input signal. As a consequence the proposed rectifier is capable to rectify all range of biological signals since as

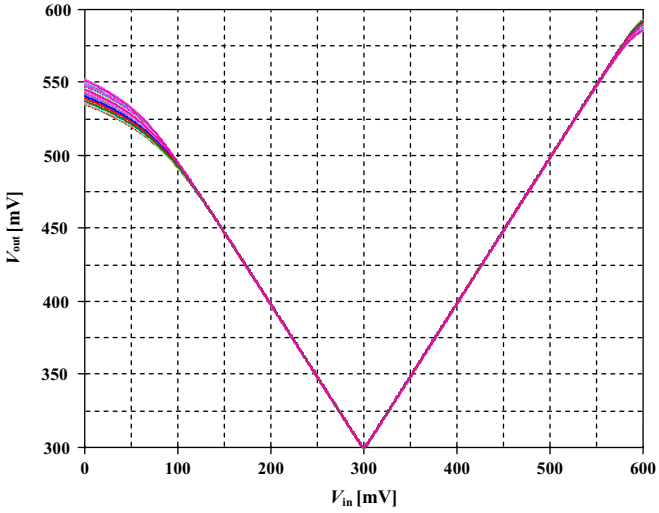

Fig. 7. Monte Carlo simulation with hundred runs for DC transfer characteristic of BD-WTA full-wave rectifier.

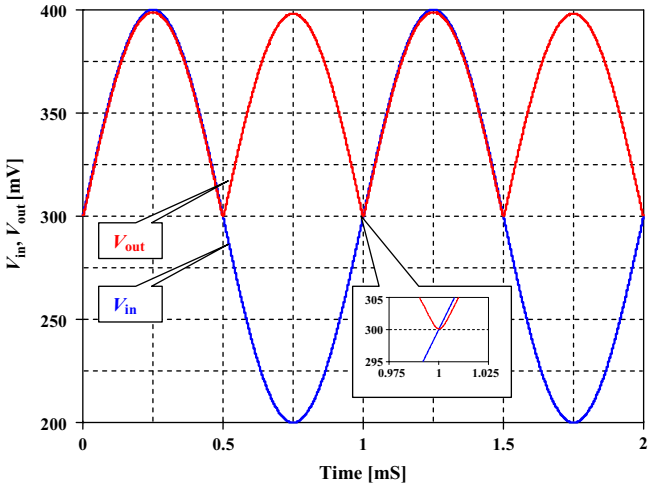

Fig. 8. Transient responses of input and output signals for 1 kHz and V_m=100 mV.

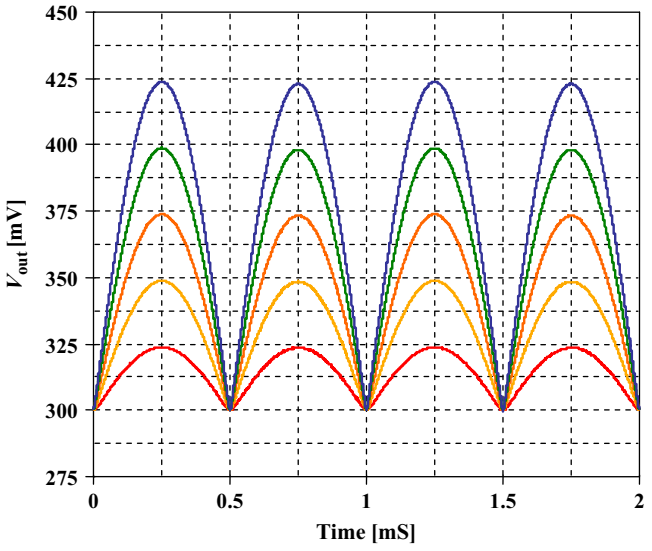

Fig. 9. Transient analyses of output waveforms with 1 kHz and various amplitudes of the input signal.

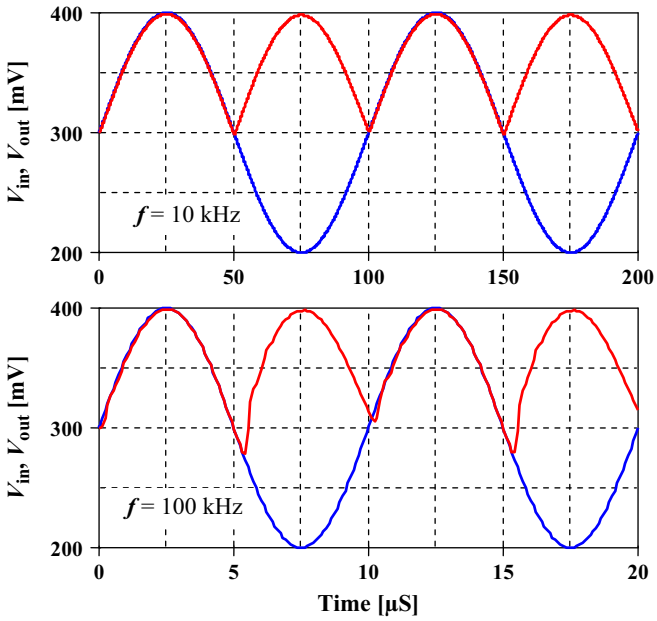

Fig. 10. Transient analyses of input and output waveforms with 10 kHz and 100 kHz and V_m = 100 mV.

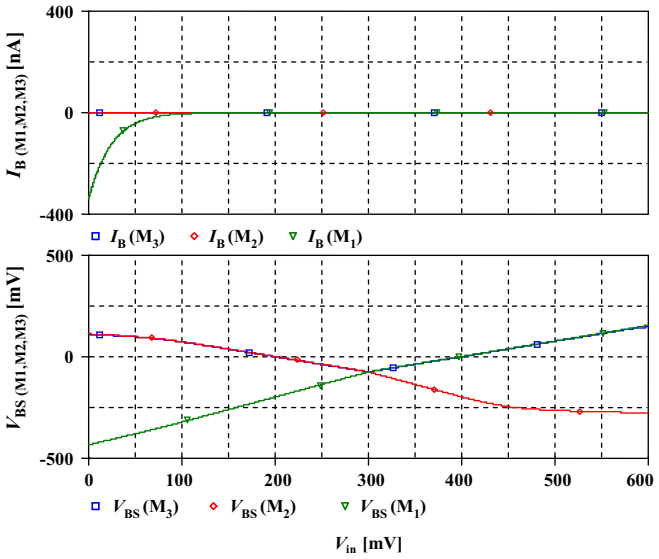

Fig. 11. The bulk-source voltage and bulk current versus input voltage.

it was mentioned before that the natural of these signals vary from a fraction of a hertz to several kilohertz.

High input impedance, which in its turns means small input current, is achieved as the bulk-source voltage (V_{BS}) of the input transistors (M_1–M_3) remains small. The input current is actually equal to the bulk current of these transistors. Therefore, in order to determine the maximum input range for satisfactory small input current (I_B), the V_{BS} as a function of the input voltage must be analyzed. It's evident from Fig. 11 that for $V_{BS} > -333$ mV the bulk current is below 7 nA, with increasing the V_{BS} above this value the bulk current increases significantly. Therefore, the maximum allowable input voltage range is [50 to 600] mV. However, since the both input terminals of the BD WTA are biased to $V_{DD}/2 = 300$ mV the amplitude of the sine wave input signal could be up to 250 mV to keep high input impedance.

To evaluate the quality of the rectification process as a function of the amplitude and the frequency of the input signal two types of characteristics are proposed [43]. The first is P_{AVR} (AVR = Average Value Ratio) which is the ratio of the average value of the rectified output signal V_{out} and the average value of the sinusoidal input signal after its ideal full-wave rectification:

$$P_{AVR} = \frac{\frac{1}{T}\int_T v_{out}(t)dt}{\frac{2}{\pi}V_m} \tag{10}$$

where T and V_m are the period and amplitude of the sinusoidal input signal. The ideal operation of the rectifier is then characterized by the value $P_{AVR} = 1$. With increasing the frequency and decreasing the amplitude of the input signal, the deviation from the ideal operation is indicated by a change, mostly a decrease in P_{AVR} below one.

The second type of characteristic is defined more rigorously as a ratio of two Root Mean Square "RMS" values, the RMS of the difference of the real and ideal output signals, v_{out} and v_{ideal}, and the RMS value of the ideal signal:

$$P_{RMSE} = \frac{\sqrt{\frac{1}{T}\int_T [v_{out}(t) - v_{ideal}(t)]^2 dt}}{\frac{1}{\sqrt{2}}V_m} \tag{11}$$

Here, the suffix RMSE is an abbreviation of the term "Root Mean Square Error". For ideal circuit operation, i.e., $v_{out}(t) = v_{ideal}(t)$, the result is $P_{RMSE} = 0$, while in the case of total attenuation of the output signal $P_{RMSE} = 1$. For extra high distortions, when the mutual energy of signals v_{out} and v_{ideal} can be negative, one can obtain $P_{RMSE} > 1$.

Fig. 12 shows the P_{AVR} (a) and P_{RMSE} (b) versus frequency in range of 1 Hz up to 200 kHz for four amplitudes of the input voltage [10, 25, 100, 150] mV. It is evident that with increasing frequency and/or decreasing the amplitudes of the input signal the P_{AVR} value decreased below the ideal unity value whereas the P_{RMSE} increased above the zero value.

Fig. 13 shows the simulated dynamic range (DR) of the rectifier for operational frequency of 1 kHz. The DR is provided for the half- and fall-wave rectifier. It is apparent that the DR of the half-wave rectifier is larger than the full-wave one because of the impact of the simple inverter. The simple inverter affects the input–output power linearity in low input powers.

Based on our survey of LV LP state-of-the-art rectifiers we found they are half-wave [15,16,18]. Therefore, in Table 2 a comparison is provided with our proposed half-wave rectifier. Three figures of merit are given to compare the rectifier's

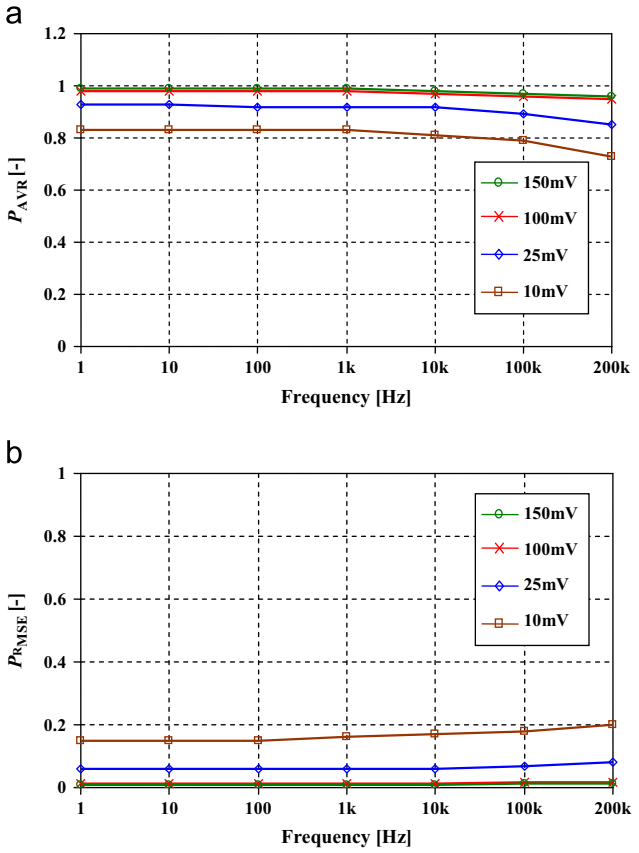

Fig. 12. AVR (Average Value Ratio) (a) and RMS error (b) versus frequency for four amplitudes of the input voltage [10, 25, 100, 150] mV.

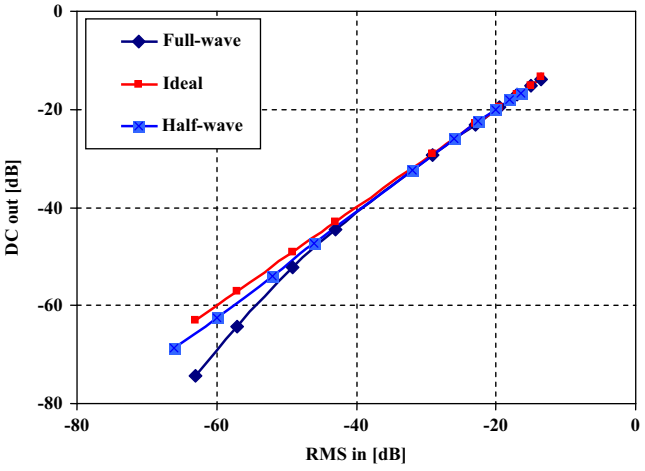

Fig. 13. DC outputs versus the RMS input for half- and full-wave rectifier.

performances. It is clear that our proposed circuit offers the lowest voltage supply and the highest FOM_3 which means the highest input swing over voltage supply. In addition the circuit offers the highest maximum frequency with the simplest CMOS internal structure using minimal number of transistors.

5. Conclusion

The paper presents a low-voltage bulk-driven rectifier based on winner-take-all circuit approach. The attractive features are the circuit simplicity, small area and high input amplitudes range. The circuit operates with the single supply of 600 mV with power consumption about 2.14 μW. It is able to handle sinusoidal signal with amplitudes up to 250 mV with a dynamic range up to 48 dB. It is capable to rectify frequencies from a fraction of a hertz to several tens of kilohertz. The proposed circuit is expected to find many applications in the biomedical area.

Table 2
Performance comparison with corresponding implementation in the literature.

Parameter		Proposed (half-wave)	[15]	[16]	[18]
Technology	μm	0.18	0.35	1.5	0.18
Supply voltage	V_{DD}[V]	0.6	1	2.8	1.8
Power consumption	P_{DD}[nW]	2140	60	2800	1080
Maximum amplitude	$V_{m.max}$[mV]	250[a]	230	850	630
Maximum frequency	f_{max}[kHz]	200[a]	0.1	10	20
Integrated input noise	v_n(μVrms)	0.19	14.6	–	–
Dynamic range	DR[dB]	48 @1 kHz	80	76	64@20 kHz
FOM_1[b]	10^6	58.7	3830	684	514
FOM_2[c]	10^{12}	23.5	16.7	22.5	29.3
FOM_3[d]	%	50	23	30	35

[a] $1 \geq P_{AVR} \geq 0.707$, $0 \leq P_{RMSE} \leq 0.2$.
[b] $FOM_1 = 10^{DR/20} V_{m.max}/(V_{DD} P_{DD})$.
[c] $FOM_2 = 10^{DR/20} f_{max}/P_{DD}$.
[d] $FOM_3 = (V_{m.max}/V_{DD})100\%$.

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