

A Comparative Study of AC/DC Converters for High-Power DC Arc Furnace

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Abstract—Today, dc arc furnaces are supplied by thyristor rectifiers. Because of the phase control strategy on the rectifiers, the arc voltage swings induce large reactive power variations on the power network and a static var compensator (SVC) or a static synchronous compensator (STATCOM) is always added to avoid flicker effect. In this paper, the authors present a new control strategy which suppress the flicker effect and increases the furnace productivity. To supply the dc arc furnace, the ac/dc converter is based on diode rectifiers and choppers with a constant power control strategy. Consequently, the ac/dc converter can operate without a STATCOM or an SVC. To evaluate the gain in flicker and furnace productivity, simulations are done with Matlab software. These simulations take into account arc voltage measurements on a 100-MW dc arc furnace and allow for comparison of the different solutions.

Index Terms—DC arc furnace, dc power supply, industrial applications, power quality, reduction of flicker effect, simulation.

I. INTRODUCTION

ELECTRICAL arc furnaces are used in the steel industry to melt scraps (35% of the world steel production). They are one of the most powerful electrical loads and they can be supplied with alternating current or direct current. The dc solution is less polluting for the power networks, regarding flicker, power factor, and harmonics [1]. Classically, for a 100-MW dc arc furnace, supplied by thyristor rectifiers with a pulse number of 24, the low-rank harmonic currents at the point of common coupling (PCC) are lower than 1% of the fundamental current [2]. The flicker effect, induced by the low-frequency modulation (between 0.5–20 Hz) of the voltage at the PCC, is the major disturbance. A static var compensator (SVC) or a static synchronous compensator (STATCOM) must be added to the thyristor rectifiers to compensate the reactive power fluctuation. The dimensioning of the SVC or STATCOM depends on the level of these fluctuations. Compared to a STATCOM, an SVC structure with thyristor-controlled reactors (TCRs) and shunt passive filters is a low-cost solution at this level of power. The STATCOM solution, based on voltage-source inverters, has a reduced volume (no passive filter) and a better response time with respect to the reactive power fluctuations. The aim of this paper is to show how it is possible to reduce the flicker effect on the power network

and to avoid the use of an SVC or a STATCOM. Compared to a STATCOM solution, which compensates the reactive power and has no effect on the furnace working, the new constant power control strategy, proposed by the authors, and applied to a diode rectifiers/choppers structure allows increasing the electrical energy transferred to the furnace. This is a major advantage for the steelmaker who can increase the furnace productivity.

II. STRUCTURE AND CONTROL OF THE DC ARC FURNACE SUPPLIES

A. Classical AC/DC Converter

Classical supplies for dc arc furnaces use full-bridge thyristor rectifiers [Fig. 1(a)] connected to medium voltage (33 kV) with special coupling transformers. This special coupling is used to get a pulse number $p = 24$ for the rectifiers. At the output, each rectifier is connected to the anodes with inductor in series. Usually, the inductor value is $250 \mu\text{H}$. The arc voltage is controlled by the cathode height and the current is controlled by the thyristor rectifiers. The switching frequency of thyristors is fixed by the frequency of the power network and then the bandwidth of the current control loop is limited. In classical supply, the operating mode is a constant current control with an average arc voltage controlled by the cathode position [3].

Fig. 2(a) shows the output waveforms for a classical supply using thyristor rectifier. In this case, the arc furnace capacity is 100 tons, and the power level is 100 MW. The scraps are charged in two times and the tap-to-tap time is about 45 min.

At $t = 0$, the first scraps basket is charged into the furnace, and we have five operating sequences.

- Sequence 1: Boring (400 V/100 kA)—During this sequence, the arc length is reduced and the average value of the electrical power is 40 MW. The cathode bores a shaft in the middle of the scraps. This shaft allows limiting the radiation of the arc on the surface of the furnace and protects the refractor. The duration of this sequence is about 2 min.
- Sequence 2: Melting (800 V/120 kA)—During this sequence, the electrical power transmitted to the arc is 100 MW. To cut the biggest scraps, oxygen hoses are used and at the end of the sequence an injection of carbon allows for melting of the final scraps.
- Sequence 3: Second basket charging (power off)—When the first basket is melted, the second basket is charged.

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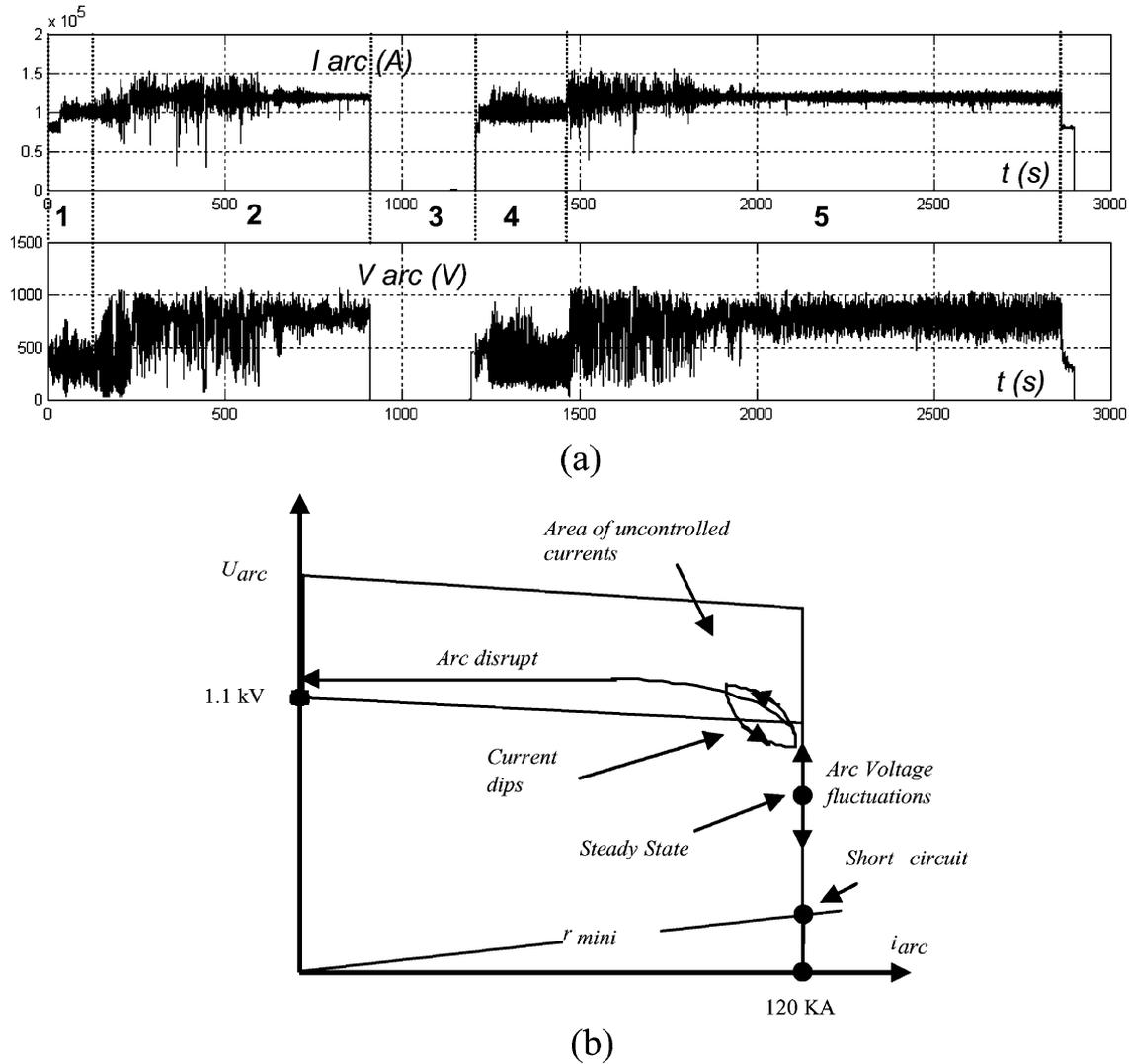


Fig. 2. (a) Current and voltage waveforms for a classical dc arc furnace. (b) Output characteristic of a classical supply.

Sequence 4: Second boring sequence (400 V/100 kA).

Sequence 5: Second melting and refining (800 V/120 kA)—When the temperature of the metal bath is equal to 1620 °C, additives are introduced into the furnace to improve the steel quality. At the end of this sequence, the melted steel is transferred in a shell to the continuous casting.

As shown in Fig. 2(a), the arc voltage variations cannot be compensated by cathode regulation because it is a heavy mechanical system with a response time of 1 s.

When the arc furnace is working, the large variations of arc voltage induce current dips, short circuits, and sometimes an arc disrupt [Fig. 2(b)]. In some cases, to avoid current dips and arc disrupts, the value of the smoothing inductors is set to 1 mH, which increases the total cost of the supply and reduces the efficiency. In any case, during the tap-to-tap time, we get large active and reactive power variations. As it shows the expression of voltage drop at the PCC (1) the reactive and active power variations induce flicker effect on the power network (V_0 is the voltage at the PCC for no load, R and X are, respectively, the

line resistance and reactance at the PCC, δP and δQ are the active and reactive power variations at the PCC)

$$\Delta V = R \frac{\delta P}{3V_0} + X \frac{\delta Q}{3V_0} \quad (1)$$

To avoid the flicker, an SVC or a STATCOM is always added to the thyristor supply [Fig. 1(a)].

B. Constant Reactive Power AC/DC Converter

To minimize the reactive power variations, it was proposed in [4] and [5] to use thyristor rectifiers with freewheel diodes working with a constant reactive power control strategy. Fig. 1(b) shows the topology of this supply using freewheel diodes connected to the neutral point of the secondary windings. To control each rectifier, two angles α_p (common cathode cell) and α_n (common anode cell) are used. These angles allow for an independent control of active and reactive power in a large working range. The control strategy with $\alpha_p \neq \alpha_n$ produces in the secondary windings of the transformers direct current and low-frequency harmonics whose ranks are defined by the following relationship:

$$h = 3k \pm 1, \quad k \in N. \quad (2)$$

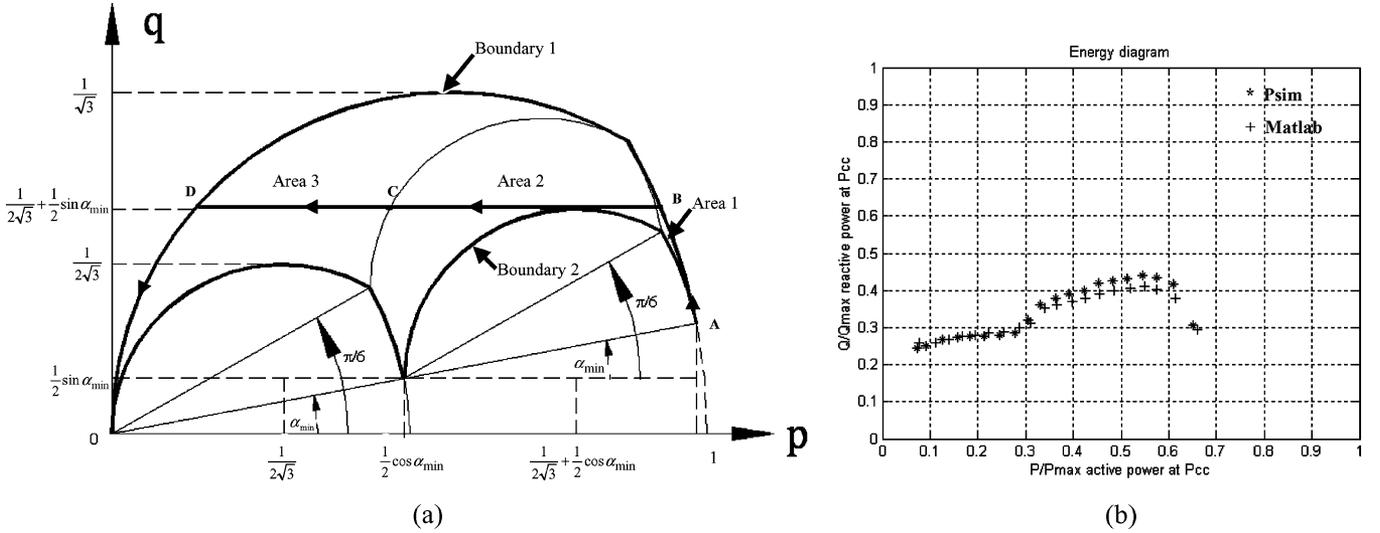


Fig. 3. Thyristor rectifier with neutral-point freewheel diodes. (a) $q = f(p)$ theoretical diagram. (b) Simulation results $q = f(p)$ diagram at PCC.

The dc and zero-sequence components can be suppressed by the means of a double secondary transformer using a delta-connected primary side. Furthermore, the even-rank harmonics are suppressed by crossing the firing angles between the two rectifiers. At the end, the ranks of current harmonics are defined by the following relationship:

$$h = 6k \pm 1, \quad k \in N. \quad (3)$$

Finally, to get a pulse number of 12 for the dc supply, a special coupling on the primary side of the transformers is used [Fig. 1(b)] (this leads to a phase shift of 30° between the secondary voltages).

Fig. 3(a) shows the $q = f(p)$ diagram for this supply. This diagram shows two boundaries B1 and B2: B1 is corresponding to the no-dissociated firing angles operating mode and B2 is corresponding to the dissociated firing angles operating mode. Between the first and the secondary boundary an operating mode at constant reactive power can be used. Assuming that overlaps are neglected, the p.u. active and reactive powers are given by the following relationships where p_p , q_p , p_n , and q_n are, respectively, the active and reactive power for the common cathode cell and the common anode cell:

$$\left. \begin{array}{l} \text{Area 1} \left\{ \begin{array}{l} p_p = \frac{1}{2} \cos(\alpha_p) \\ q_p = \frac{1}{2} \sin(\alpha_p) \\ p_n = \frac{1}{2} \cos(\alpha_n) \\ q_n = \frac{1}{2} \sin(\alpha_n) \end{array} \right. \\ \text{Area 2} \left\{ \begin{array}{l} p_p = \frac{1}{2\sqrt{3}} \left[\cos\left(\alpha_p + \frac{\pi}{6}\right) \right] \\ q_p = \frac{1}{2\sqrt{3}} \left[\sin\left(\alpha_p + \frac{\pi}{6}\right) \right] \\ p_n = \frac{1}{2} \cos(\alpha_n) \\ q_n = \frac{1}{2} \sin(\alpha_n) \end{array} \right. \\ \text{Area 3} \left\{ \begin{array}{l} p_p = \frac{1}{2\sqrt{3}} \left[1 + \cos\left(\alpha_p + \frac{\pi}{6}\right) \right] \\ q_p = \frac{1}{2\sqrt{3}} \left[\sin\left(\alpha_p + \frac{\pi}{6}\right) \right] \\ p_n = \frac{1}{2\sqrt{3}} \left[1 + \cos\left(\alpha_n + \frac{\pi}{6}\right) \right] \\ q_n = \frac{1}{2\sqrt{3}} \left[\sin\left(\alpha_n + \frac{\pi}{6}\right) \right] \end{array} \right. \end{array} \right\} \quad (4)$$

By inverting the equation system for each area, it is possible to calculate the firing angles α_p and α_n to get a control of the converter with constant reactive power (straight line BD).

This supply allows for a reduction of the flicker effect and a better power factor than a classical supply, but it keeps the same limits in the output characteristic as in Fig. 2(b). Consequently, the control of output current and active power on electrical arc is not optimal.

C. Indirect AC/DC Converter With High-Power Choppers and Constant Power Control

1) *Topology of the AC/DC Converter:* To avoid the flicker effect on the power network by reducing the active and reactive power variations, we proposed in [6] an indirect ac/dc structure with high-power chopper associated with a new control strategy [Fig. 1(c)]. Compared to the topology presented in [7], Fig. 1(c) shows a matrix layout of the rectifiers/choppers.

The advantages of our topology are: effective balancing of the currents on each transformer secondary winding and easy matching for different power levels and number of anodes. The matrix layout insures a power distribution on each rectifier and current control loops are used to distribute the current between the dc/dc converters. Furthermore, the current balancing on each transformer secondary allows for suppression of low-rank harmonics and harmonics filters on the high-voltage side are not necessary.

At this level of power (100 MW), the transformer short-circuit impedance is about 15% ($r_{sc} = 0,1 \text{ m}\Omega$; $\lambda_{sc} = 8,7 \mu\text{H}$) and it is not necessary to add an inductor on the dc side. At the output of the rectifiers, each capacitor bank has a value of 84 mF. Simulations waveforms (PSIM software) are shown in Fig. 4.

At the medium-voltage side ($U = 33 \text{ kV}$), the power factor of the dc supply is 0.93 for $P = 100 \text{ MW}$ (melting phase) and 0.97 for $P = 40 \text{ MW}$ (boring phase). For the input currents, low-rank harmonics are suppressed up to rank 19. The total harmonic distortion (THD) is 1.16% for $P = 100 \text{ MW}$ and 2.12% for $P = 40 \text{ MW}$. It should be noted that, for each rectifier, the input current THD is 29.8% for $P = 100 \text{ MW}$ and 44.2% for

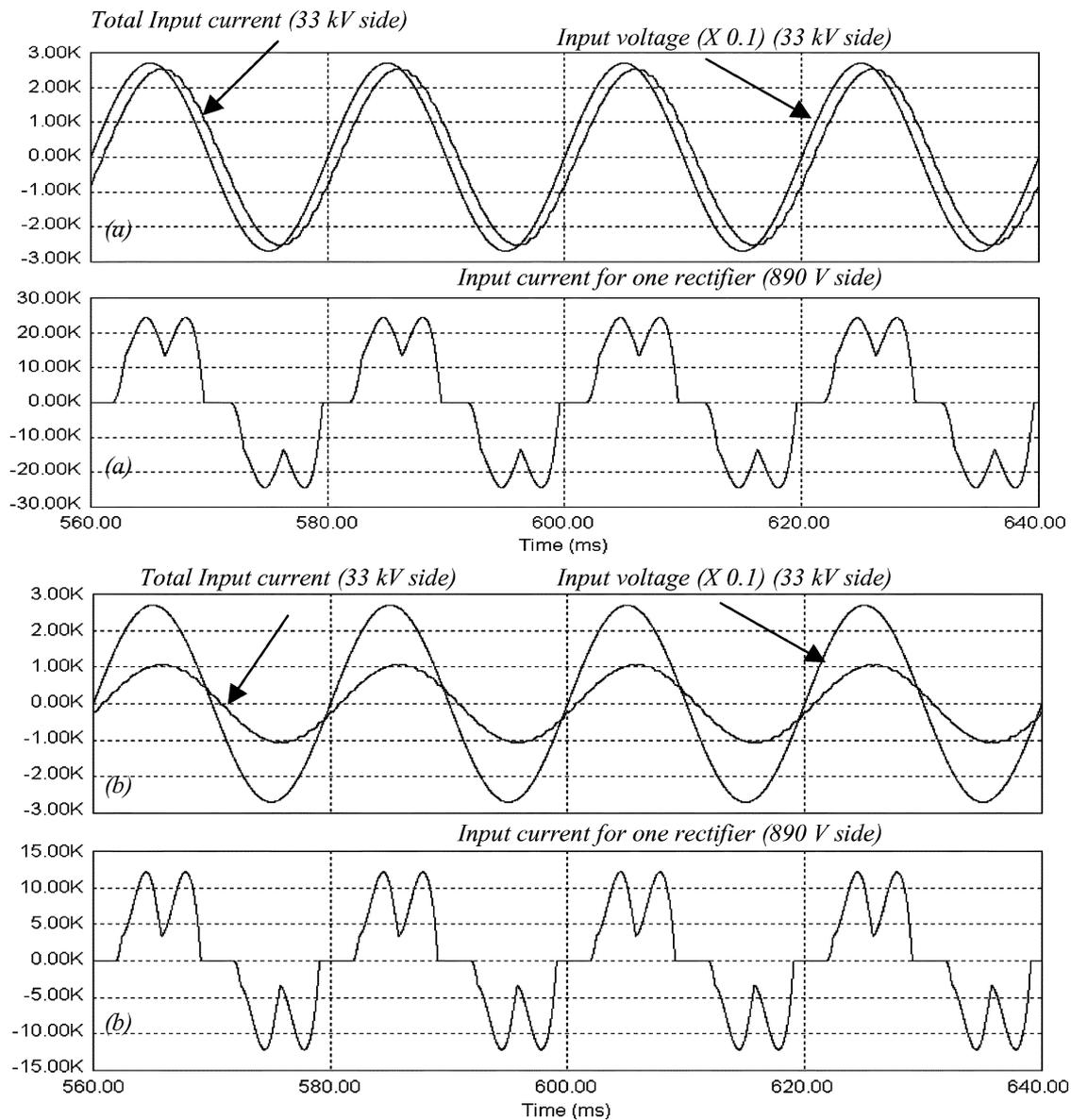


Fig. 4. Diode rectifiers input waveforms. (a) $P = 100$ MW. (b) $P = 40$ MW.

$P = 40$ MW. At this level of power (100 MW), the use of an active rectifier (with PWM control), will be too expensive to achieve unity power factor.

2) *Control Strategy of the AC/DC Converter*: If a constant current control is used on the choppers, the output characteristic of the supply is the same as a classical structure with thyristor rectifiers [Fig. 2(b)]. The reactive power on the network is reduced, but the large variations of the arc voltage will always induce current dips, short circuits, and sometimes arc disrupts. The simulation results presented in Fig. 5(a) and (b) allow for a comparison of the thyristor rectifier solution and the chopper solution. For the chopper solution, the reactive power variations are reduced, but the active power variations are the same as the classical solution.

To reduce flicker effect on the power network [3], we propose using a constant power control on the choppers (Fig. 6). Thanks to the high switching frequency on the choppers (1 kHz), it is possible to follow the arc voltage fluctuations and achieve really

constant active and reactive power on the network except during a short circuit.

During a short circuit, the current is limited to 1.5 times the nominal value which is acceptable by the cathode during a few seconds. Fig. 5(c) shows simulation results for the chopper solution in the case of constant power control. The reactive power consumed by the dc supply is only the reactive power of the transformer (leakage inductor) and the input power factor is equal to 0,93 (see the waveforms of Fig. 4).

3) *Topology and Design of Elementary DC/DC Converter*: Fig. 7 shows a buck converter composed of three chopper legs. The dc-bus voltage is fixed at 1.2 kV and semi-conductors with a minimum of 2.5-kV sustaining voltage are used. As we have seen in Section II [Fig. 2(a)], standard furnaces use two voltage levels: 400 V for the boring sequence and 800 V for the melting sequence. To reduce the input and output current ripple the control signals of the three chopper legs are interleaved. In this case, a number of chopper legs (multiple

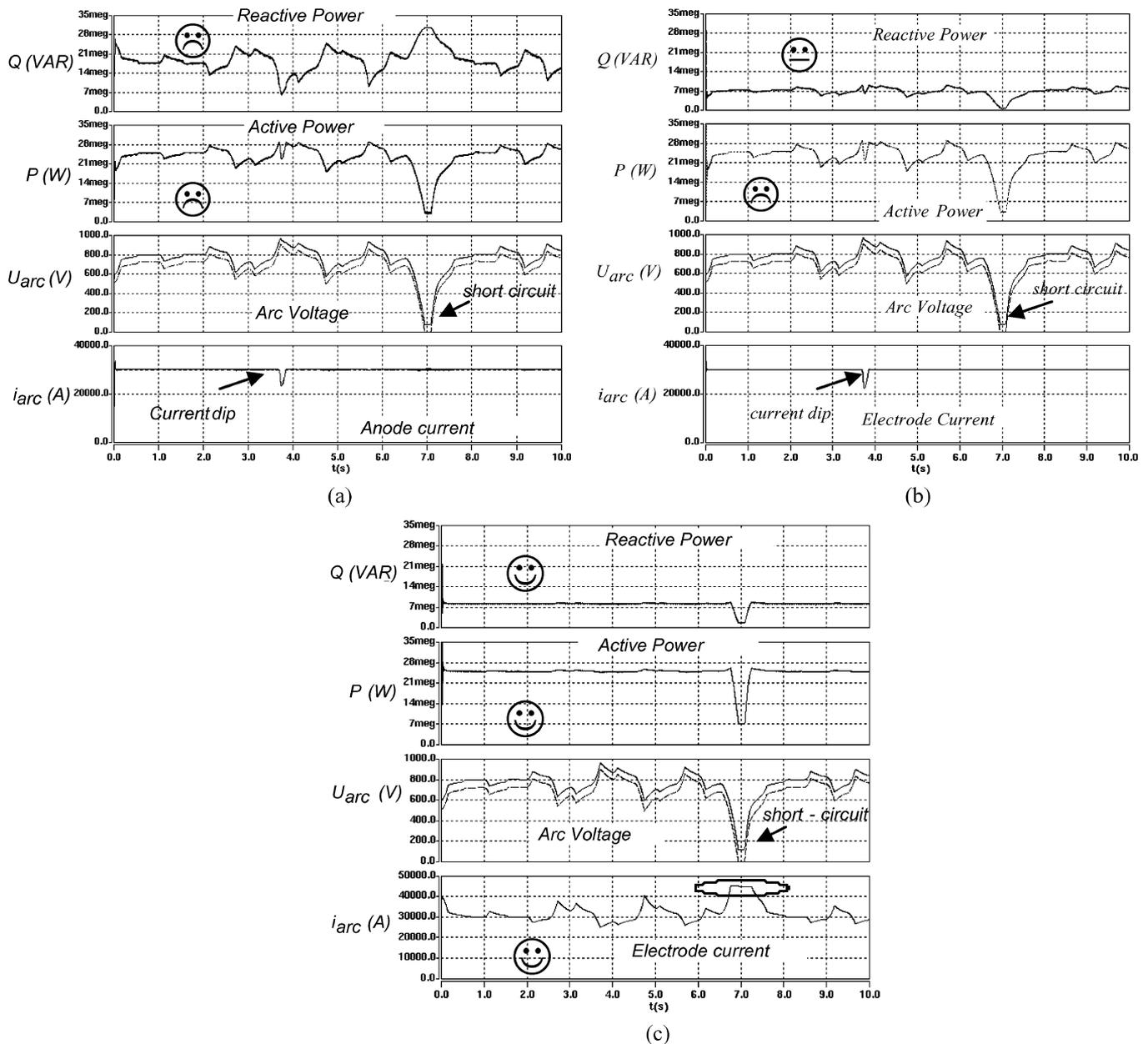


Fig. 5. Simulation waveforms for one anode. (a) Classical supply with thyristor rectifiers. (b) Chopper solution with constant current control. (c) Chopper solution with constant power control.

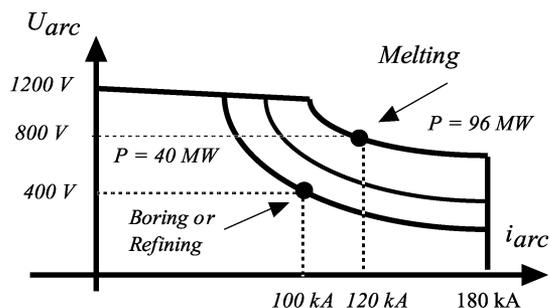


Fig. 6. Output characteristic of the chopper dc supply during the tap-to-tap time.

of three) allows for an output current ripple equal to zero for the nominal working points (boring sequence $V_{in} = 1200$, $V_{out} = 400$ $\delta = 1/3$, and melting sequence $V_{in} = 1200$, $V_{out} = 800$ $\delta = 2/3$).

To have a matrix layout [Fig. 1(c)], the number of elementary dc/dc converters (buck converter in parallel association) should be a multiple of 16 (4 rectifiers \times 4 anodes), therefore, the number of chopper legs should be a multiple of 48 (16 \times 3) to cancel the current ripple for the nominal output voltage (800 V). To find the minimum number of chopper legs for an output power of 100 MW, it is necessary to evaluate the losses in the semiconductors and to consider the junction temperature variations induced by arc voltage swings.

For this high-power application, integrated gate-commutated transistor (IGCT) and integrated gate bipolar transistor (IGBT) solutions were considered. Compared to IGBTs, IGCTs have low on-state voltage and accept larger variations for the junction temperature, but their switching losses are greater. For the design, the junction temperature calculation was based on semiconductor data sheets. For the IGBTs chopper, the

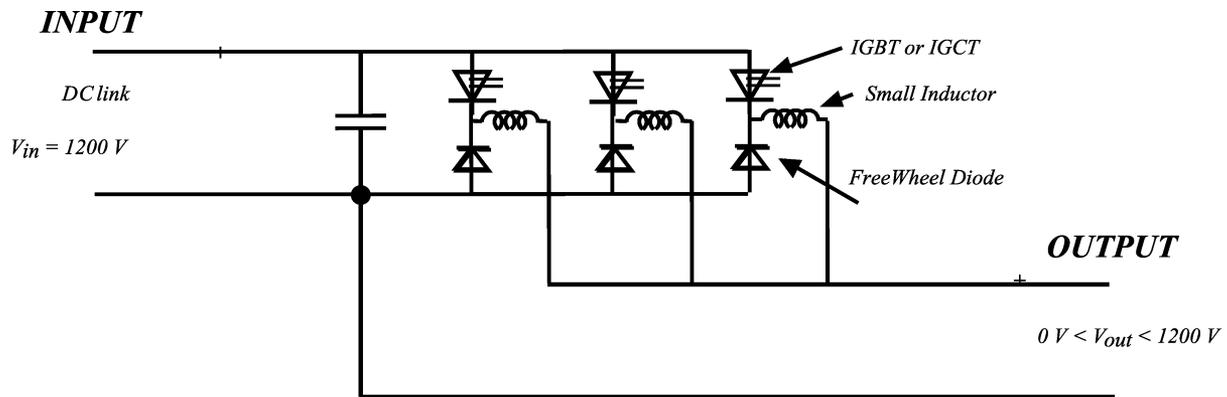
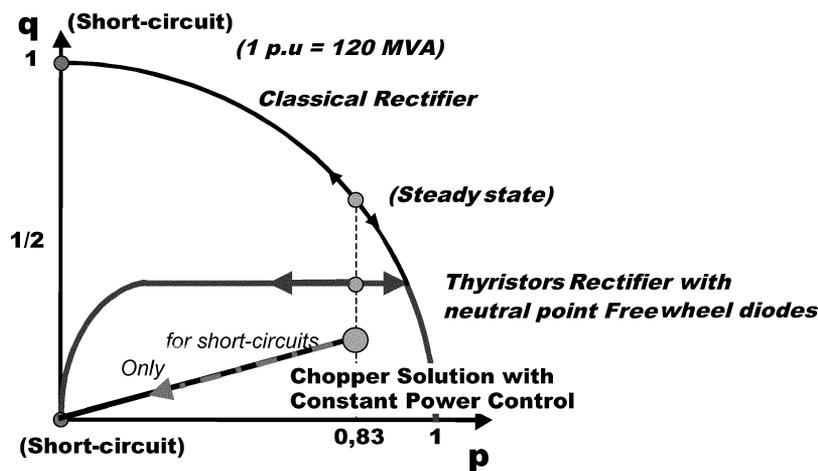


Fig. 7. Buck converters in parallel association.

Fig. 8. Reactive power versus active power ($q = f(p)$).

controlled switches reference is: FZ 1500 R25 KF1 (EUPEC) and the diode reference is: DD 1200 S33 K2 (EUPEC). For the IGCTs chopper, the controlled switch reference is: 5SHY 35L4510 (ABB) and the diode reference is: 5SDF 16L4502 (ABB).

For a cycles number of 20 000 000, IGBTs accept a $\Delta T_{j \max}$ of 34 °C and IGCTs accept a $\Delta T_{j \max}$ of 45 °C [6]. The design method and the simulation results were detailed in [6] and it was theoretically shown that, for the same life time (20 000 000 cycles), IGBT and IGCT solutions are equivalent. For a 100-MW arc furnace and with a switching frequency of 1 kHz, the minimum number of chopper legs is equal to 156. Finally, the new dc supply will include 64 high-power chopper blocks including an input capacitor of 5.2 mF and three output inductors of 750 μ H. Two prototypes of chopper blocks were tested to validate the design and to compare the IGBT and IGCT solutions. The test results published in [8] clearly show an advantage for the IGCT solution with respect to the thermal cycling.

III. COMPARISON BETWEEN THE DC SUPPLY WITH CONSTANT POWER CONTROL, AND THE THYRISTOR SUPPLIES

In this section, the solutions are compared with two points of view: the flicker induced at the PCC and the electrical power transferred to the arc.

A. Evaluation of Flicker Effect

Fig. 8 shows, at the primary side of the transformers, the $q = f(p)$ diagrams for the three supplies. For the new dc supply the reactive power variations are limited: the $q = f(p)$ diagram is represented by only one working point except when a short circuit occurs.

Another advantage of the constant power control is the power rating of the transformers. For the thyristor supplies, with constant current control, a voltage margin is taken to avoid current dips and arc disrupts [Fig. 2(b)]. This leads to having a steady-state point in the $q = f(p)$ diagram with a high level of reactive power and the transformers must be oversized. In the case of the new dc supply, due to the constant power control, the voltage margin does not induce an oversizing of the transformers which are rated only for the active power.

To determine the flicker effect, the simulations have been carried out with MATLAB/SIMULINK software. A typical plant, supplied by a 220-kV line, is considered [Fig. 9(a)]. For the lines and the transformers, all the resistors and inductors are taken into account. At the input of the ac/dc converter (890 V), the total impedance of the voltage source is characterized by: $L_{\text{tot}} = 13 \mu$ H and $R_{\text{tot}} = 60 \mu\Omega$.

For the simulations, arc voltage variations are read in a file including arc voltage measurements for a 100-MW arc furnace with a sampling period of 4 ms. Each converter is simulated

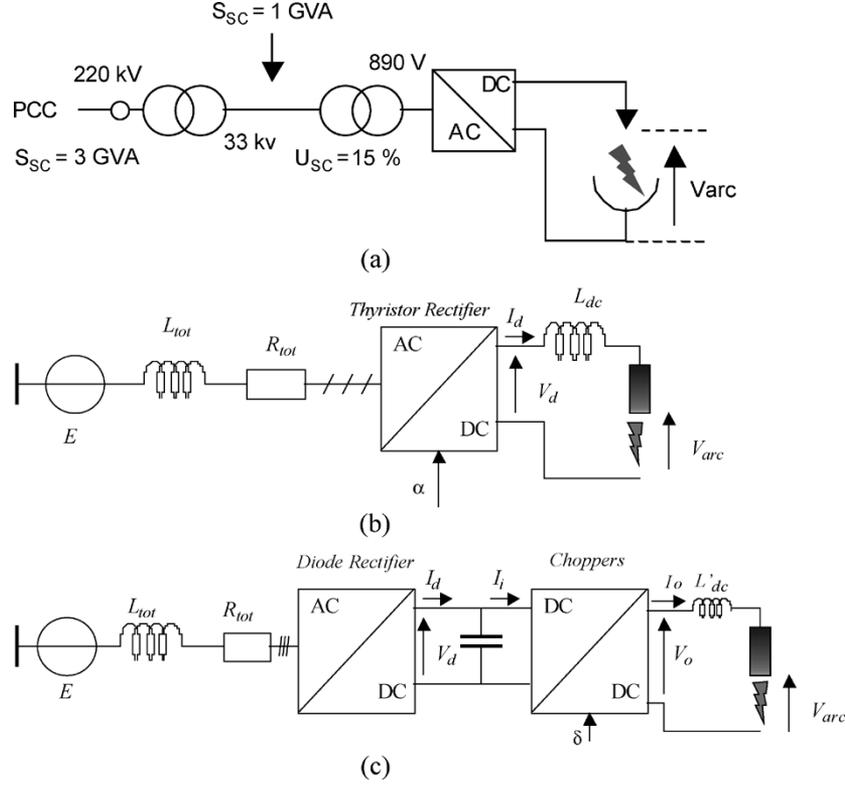


Fig. 9. (a) Structure of power supply for a dc arc furnace. (b) Equivalent circuit for one thyristor rectifier. (c) Equivalent circuit for one diode rectifier associated with choppers.

with MATLAB/SIMULINK by a quasi-static model including the current control loops: the output current ripple is neglected but average value variations are taken into account [9]. The mathematical model (power network, converter, control loops) implemented in MATLAB/SIMULINK, has been validated in PSIM software. PSIM software processes simulation with instantaneous waveforms and takes into account the control loops. The validation of averaged model implemented in MATLAB/SIMULINK was done by the comparison of the reactive and active power at PCC for different steady-state points. For example, Fig. 3(b) shows for the Q constant supply, the simulation results with PSIM and MATLAB software (at the PCC, the reactive power is not constant because of cables and transformers inductors).

1) *Averaged Model for Classical Supply With Thyristor Rectifiers*: The mean value of the output voltage of the thyristor rectifier is given by

$$V_d = \frac{3\sqrt{3}E_{\max}}{\pi} \cos(\alpha) - \frac{3}{\pi} \omega L_{tot} I_d - 2R_{tot} \cdot I_d - 2L_{tot} \frac{dI_d}{dt} \quad (5)$$

where α is the firing angle of the thyristors and I_d the averaged value of the output current [Fig. 9(b)].

The relationship between V_d and V_{arc} is

$$V_d = L_{dc} \frac{dI_d}{dt} + V_{arc}. \quad (6)$$

The overlap angle is calculated by

$$\mu = \cos^{-1} \left(\cos \alpha - \frac{2L_{tot} I_d}{\sqrt{3}E_{\max}} \right) - \alpha. \quad (7)$$

Then, the expression of the input current is given by ($e(t)$ is taken as phase reference)

$$I_L \equiv \frac{2\sqrt{3}}{\pi} I_d \sin \left(2\pi f - \alpha - \frac{\mu}{2} \right). \quad (8)$$

By referring to (8), the voltage at the PCC is easily calculated.

2) *Averaged Model for the Q Constant Supply*: The input active and reactive powers are obtained by the following relationship where α_p et α_n are calculated to insure a constant reactive power in areas 2 and 3 [Fig. 3(a)]

$$\begin{cases} p = p_p + p_n = f(\alpha_p, \alpha_n) \\ q = q_p + q_n = g(\alpha_p, \alpha_n). \end{cases} \quad (9)$$

The expression of the line current at the PCC is given by the relationship

$$I_L = 2 \frac{\sqrt{3}}{\pi} I_d \left[\sqrt{p_p^2 + q_p^2} \sin \left(\omega t + \tan^{-1} \left(\frac{p_p}{q_p} \right) \right) + \sqrt{p_n^2 + q_n^2} \sin \left(\omega t + \tan^{-1} \left(\frac{p_n}{q_n} \right) \right) \right]. \quad (10)$$

The overlaps, corresponding to the switching time of thyristors and diodes, induce a phase shift of the fundamental current and a voltage drop on the dc side. Consequently, the control angles (α_p, α_n) and then the input active and reactive powers are modified by the controller of the current loop which compensates the voltage drop. At the end, the expression of the line current is given by the following relationship where μ_n and μ_p are the overlap angles of the cells:

$$I_L = 2 \frac{\sqrt{3}}{\pi} I_d \left[\sqrt{p_p^2 + q_p^2} \sin \left(\omega t + \tan^{-1} \left(\frac{p_p}{q_p} \right) + \frac{\mu_p}{2} \right) + \sqrt{p_n^2 + q_n^2} \sin \left(\omega t + \tan^{-1} \left(\frac{p_n}{q_n} \right) + \frac{\mu_n}{2} \right) \right]. \quad (11)$$

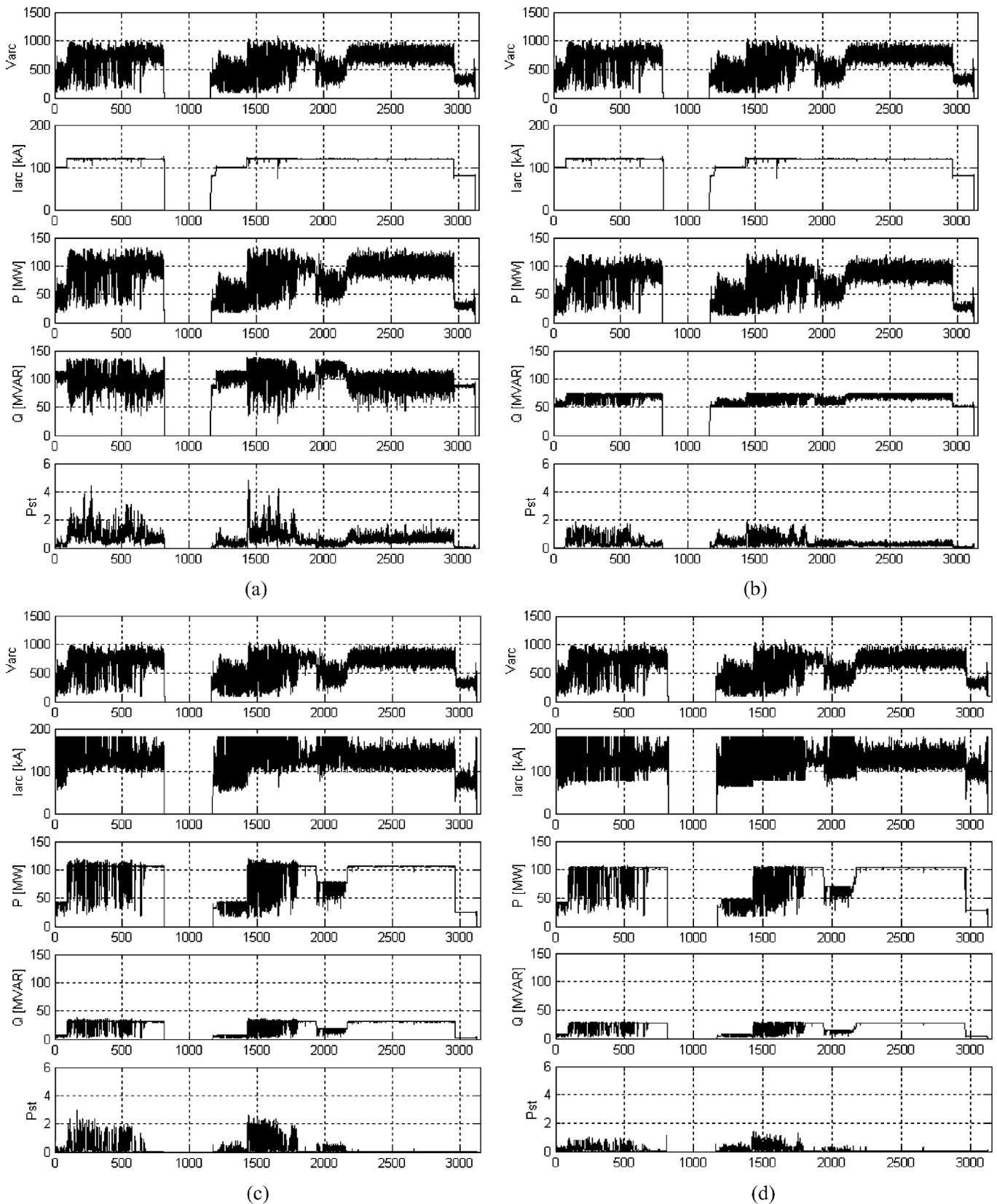


Fig. 10. (a) Simulation results for the classical supply with thyristor rectifiers. (b) Simulation results for the Q constant supply. (c) Simulation results for the chopper dc supply with constant power control. (d) Simulation results for the chopper dc supply with hysteresis on constant power control.

3) *Averaged Model for the DC Supply With Choppers*: Assuming the current I_d is always greater than zero, the equations for the diode rectifier are the same as the thyristor

rectifier with $\alpha = 0$ [see (5), (7), and (8)]. For the choppers, the relationship between input and output are

$$V_o = V_d \cdot \delta \quad (12)$$

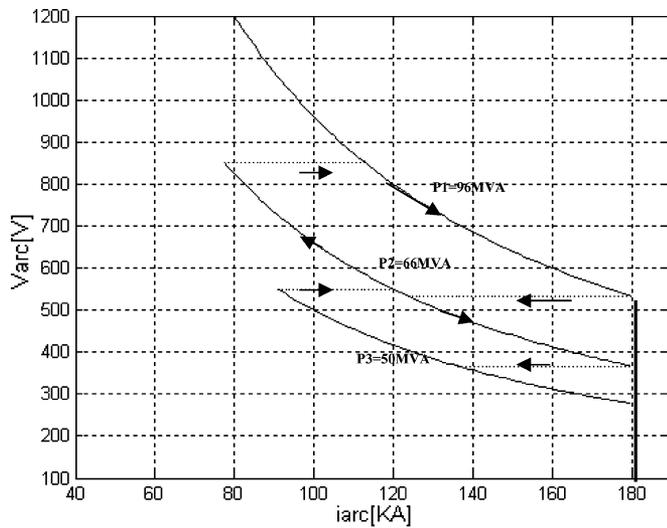


Fig. 11. Constant power control with hysteresis.

and

$$I_i = I_o \cdot \delta \quad (13)$$

where δ is the duty cycle of the control signal of the switches [Fig. 9(c)].

4) *Simulation Results:* A flickermeter, with the four classical blocks [10]–[12], has been implemented in MATLAB/SIMULINK. The Pst is approximated with respect to the output of block 4 by the relationship

$$\text{Pst} = 0.7\sqrt{\text{Out4}} \quad (14)$$

The simulations are done with the same arc voltage variations. The different phases of the tap-to-tap time are taken into account: for the dc supply with choppers, during the boring, the power reference is set to 40 MW (Fig. 6). The average voltage is always controlled by the arc length (cathode regulation).

The simulation results are presented in Fig. 10: Pst, active power, and reactive power are calculated at the PCC. As shown in Fig. 10(c), there is low reactive power consumption with the new supply and the active and reactive powers are constant except during the short circuit (note that the Pst is equal to zero when active and reactive power are constant).

5) *Constant Power Control With Hysteresis:* With the chopper dc supply, the values of the Pst are reduced but not sufficiently to suppress the SVC. By analyzing the voltage drop at the PCC (1), it is possible to show that the effect of active power variations cannot be neglected. With a view to achieve a Pst lower to or equal to 1, we propose using a constant power control with hysteresis (Fig. 11).

The simulations results are presented in Fig. 10(d); in this case, the Pst 99% is equal to 0.94 and the SVC can be suppressed.

B. Evaluation of Energy Transmitted to the Electrical Arc and Comparative Balance

With a view to evaluate the efficiency of the constant power control, measurements on a 100-MW dc arc furnace have been made. Voltage and current on the electrical arc have been stored with a sampling period of 4 ms. On the one hand, the electrical

TABLE I
COMPARISON BETWEEN THE DIFFERENT SOLUTIONS

	<i>Classical supply</i>	<i>Q constant Supply</i>	<i>Chopper solution with constant power control</i>	<i>Chopper solution with hysteresis on constant power control</i>
<i>Pst 99%</i>	2.31	1.35	1.77	0.94
<i>Energy</i>	207.19 GJ	207.19 GJ	223.06 GJ	212.01 GJ
<i>Gain</i>	0 %	0 %	7.6 %	2.3 %

energy is calculated during the tap-to-tap time with the sampled values. On the other hand, with the same arc voltage, a new current is calculated by taking into account the constant power control. Then, a new value of the energy during tap-to-tap time is estimated

With the constant active power control a significant gain is achieved on the furnace electrical energy, but with respect to flicker, the Pst is greater than one and then the constant active power control is less efficient than the constant reactive power control. With the hysteresis active power control, we obtain a compromise: the Pst is lower than one (no SVC) and the gain on the energy is 2.3% (Table I). Furthermore, in this case, assuming a furnace productivity proportional to the electrical energy transmitted to the arc, the financial gain is about 0.7 million Euro per year.

IV. CONCLUSION

This paper has presented an overview of the high-power rectifiers converters to supply electrical arc furnaces. A rectifier/chopper topology with constant power control has been proposed. It was shown that, to eliminate the flicker effect, it is necessary to work with constant active and reactive power. During the boring and at the beginning of the melting, it is not possible to satisfy this condition because of short circuits inside the furnace. The hysteresis control on the power reference allows limiting dP/dt and dQ/dt and then reduces the flicker effect to an acceptable level. With this new strategy, there are no harmonics filters on the network, and any SVC or STATCOM, and the total cost of the structure is estimated close to the thyristor solution including the SVC. Finally, the major advantage will be for the steelmaker who enjoys a better productivity of the furnace.

REFERENCES

- [1] A. Robert and M. Couvreur, *Arc Furnace Flicker Assessment and Mitigation*. Amsterdam, The Netherlands: PQA, 1994.
- [2] T. Miyashita, N. Ao, and Y. Mikami, "Development and operation of large DC arc furnace," presented at the Electrotech'92, Montreal, QC, Canada, Jun. 1992.
- [3] S. Alameddine and B. Bowman, "Electrical particularities of the melt-down in DC furnace," presented at the Int. Conf. New Developments in Metallurgical Process Technology, Düsseldorf, Germany, Jun. 1999.
- [4] F. Richardeau, Y. Cheron, J. Du Parc, M. Wursteisen, and C. Glinski, "New strategy of control at low flicker level for DC electrical arc furnace," presented at the IEEE Int. Conf. Industrial Technology, Gangzhou, China, Dec. 1994.
- [5] C. Morettin, S. Dallenogare, and J. Du Parc, "Minimum network disturbances for DC EAF using a free wheeling diode rectifier," presented at the Int. Conf. New Developments in Metallurgical Process Technology, Düsseldorf, Germany, Jun. 1999.

- [6] P. Ladoux, C. Bas, H. Foch, and J. Nuns, "Structure and design of high power chopper for DC arc furnace," presented at the EPE-PEMC, Dubrovnik, Croatia, Sep. 2002.
- [7] V. Scaini and T. Ma, "High current DC chopper in the metals industry," in *Conf. Rec. IEEE-IAS Annu. Meeting*, vol. 4, Oct., 8–12 2000, pp. 2629–2636.
- [8] S. Alvarez, P. Ladoux, J. M. Blaquiere, J. Nuns, and B. Riffault, "Evaluation of IGBT's and IGBT's choppers for DC electrical arc furnaces," *EPE J.*, vol. 14, no. 2, May 2004.
- [9] W. Hammer, "Dynamic modeling of HVDC converters," presented at the EPE 2001, Graz, Austria, Sep. 2001.
- [10] *Flickermeter Functional and Design Specifications*, IEC Standard 61000-4-15. EMC-Part 4, Rev. IEC 868, 1997.
- [11] *IEC Flickermeter Used in Power System Voltage Monitoring*, Test Protocol, UIE WG2 Power Quality and Cigre 35.05/CIRE2—CC02 Voltage Quality Working Group, Draft, Jan. 2001.
- [12] C. Hennerbichler and G. Brauner, "Universal analysis and prognosis of flicker in distribution network," presented at the PCIM'00, Nürnberg, Germany, Jun. 2000.



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